EE 330
Lecture 39

Digital Circuits

Ratio Logic
Other MOS Logic Families
Propagation Delay – basic characterization
Device Sizing (Inverter and multiple-input gates)

Exam Schedule

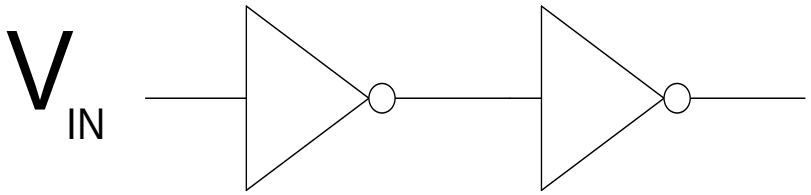
Exam 1	**Friday Sept 24**
Exam 2	**Friday Oct 22**
Exam 3	**Friday Nov 19**
Final	**Tues Dec 14 12:00 p.m.**

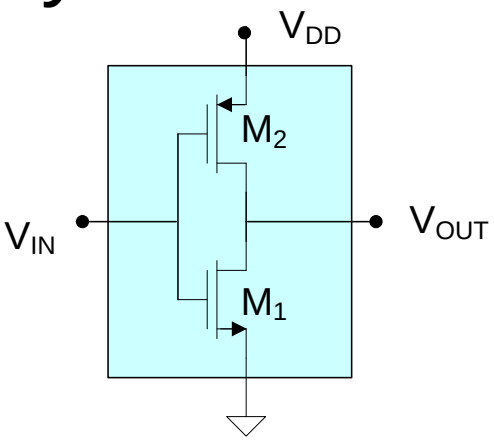
As a courtesy to fellow classmates, TAs, and the instructor

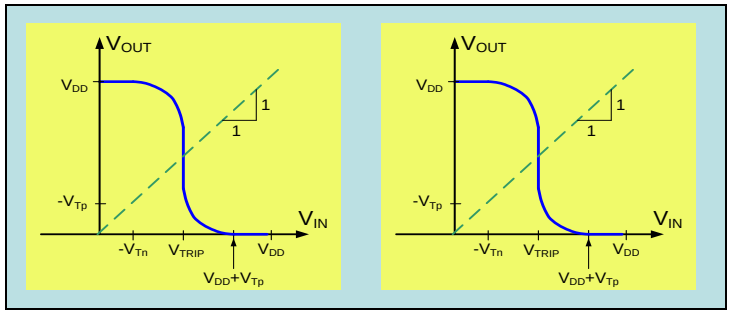
Wearing of masks during lectures and in the laboratories for this course would be appreciated irrespective of vaccination status

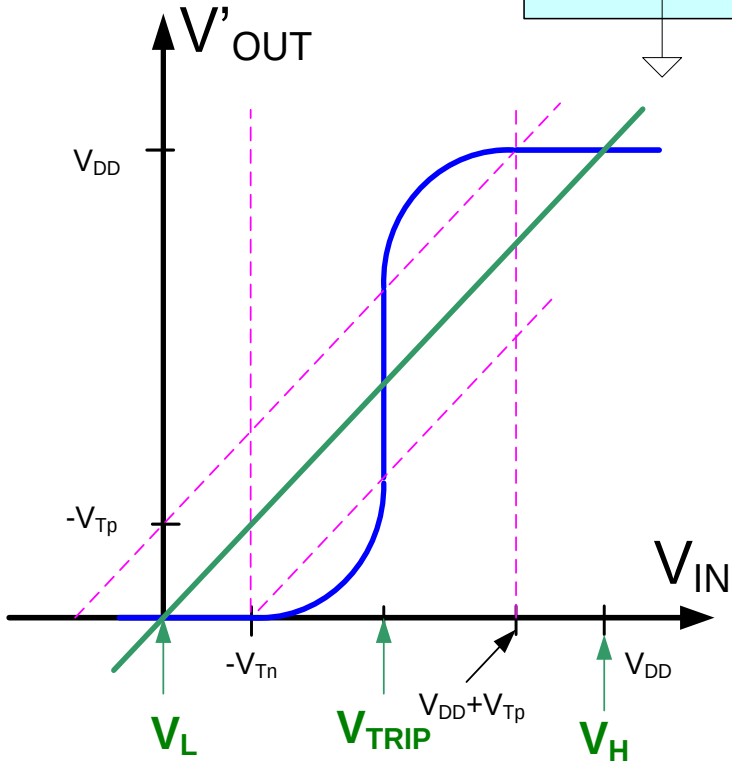
Review from last lecture

Inverter Transfer Characteristics of Inverter Pair for THIS Logic Family









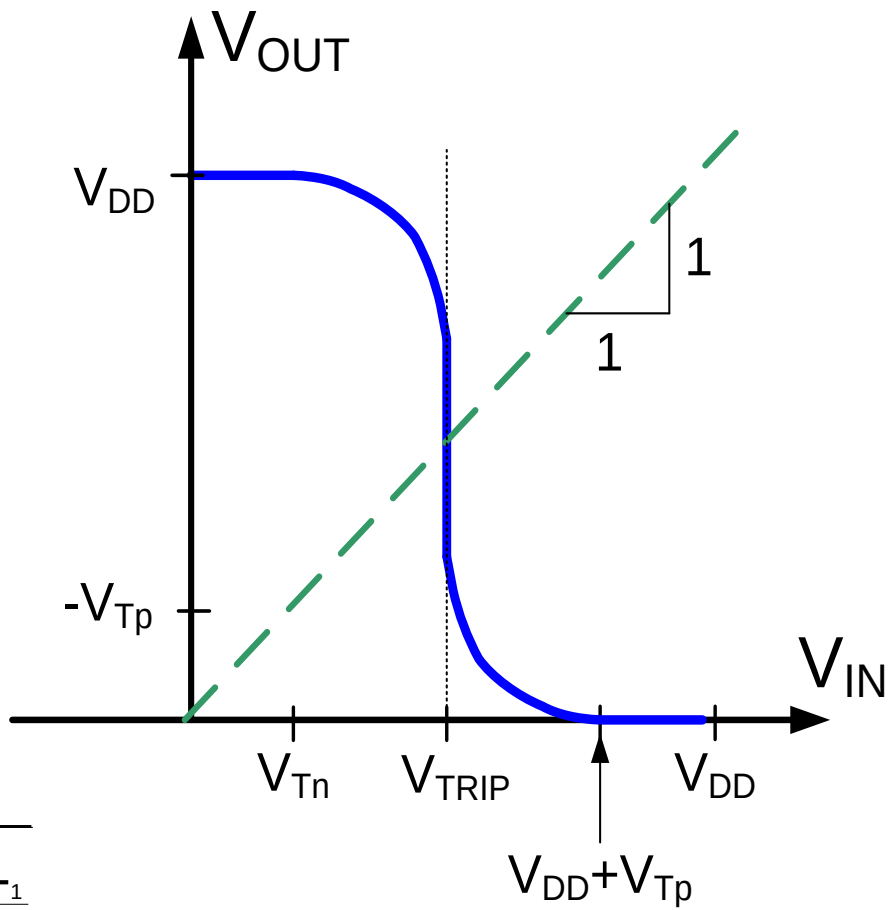
$V_H = V_{DD}$ and $V_L = 0$

Note this is independent of device sizing for THIS logic family !!

Review from last lecture

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)



From Case 3 analysis:

$$V_{IN} = \frac{\left(V_{Tn}\right) + \left(V_{DD} + V_{Tp}\right)\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}{1 + \sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}$$

Review from last lecture

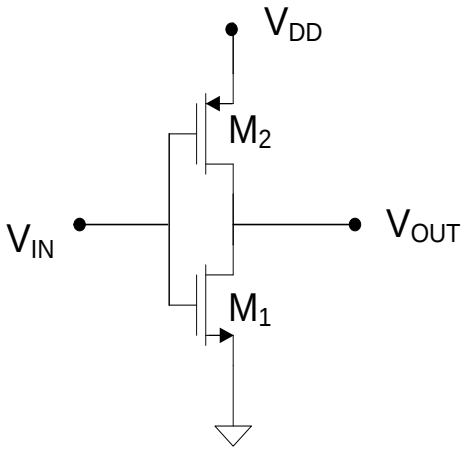
How should M_1 and M_2 be sized?

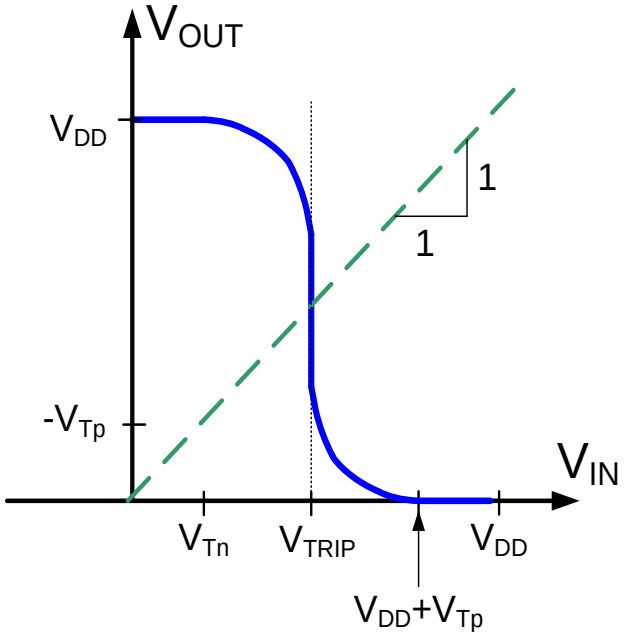
Pick $L_1=L_2=L_{min}$

<u>One</u> popular sizing strategy:

1. **Pick $W_1=W_{MIN}$ to minimize area of M_1**
2. **Pick W_2 to set trip-point at $V_{DD}/2$**

Observe Case 3 provides expression for V_{TRIP}





Summary: $V_{TRIP} = \frac{V_{DD}}{2}$ **sizing strategy**

$L_1=L_2=L_{min}$

$W_1=W_{MIN}$

$$W_2 = \frac{\mu_n}{\mu_p} W_{MIN} \simeq 3W_{MIN}$$

(dependent upon assumption $V_{Tp}= -V_{Tn}$)

Other sizing strategies will be discussed later !

Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
    - FI/OD
    - Logical Effort
  - Elmore Delay
- Sizing of Gates
  - The Reference Inverter
- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators

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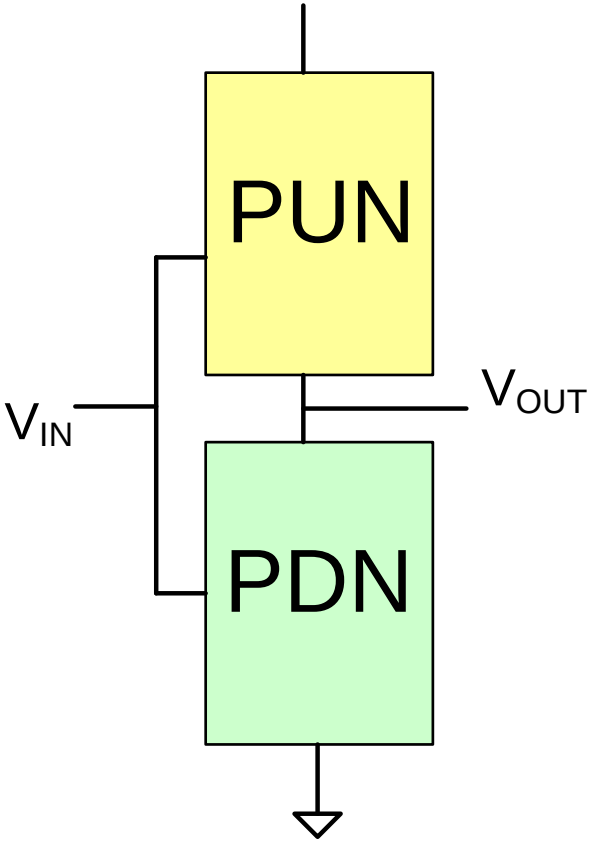
done

partial

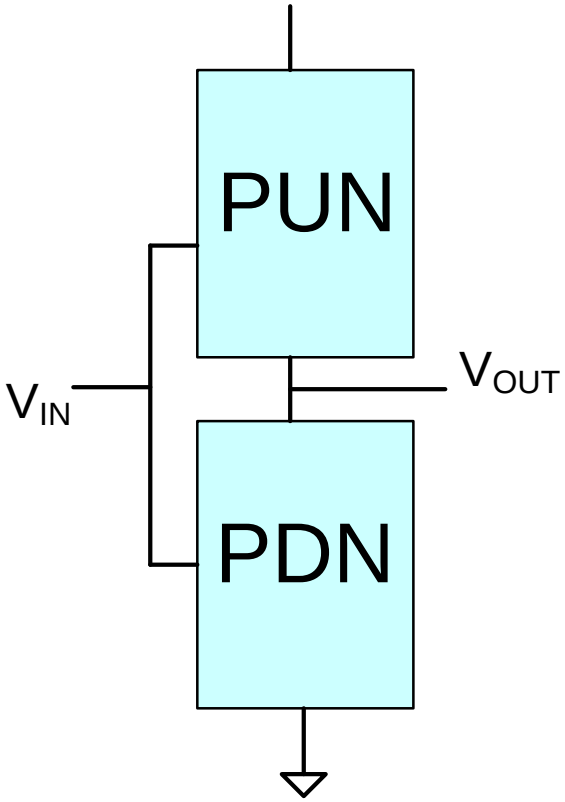
General Logic Family



Compound Gate in CMOS Process

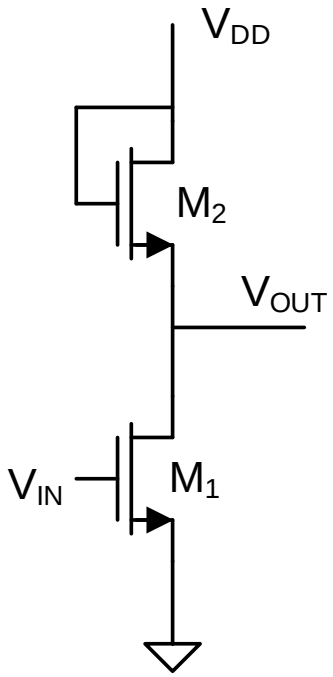
p-channel PUN
n-channel PDN

$V_H=V_{DD}$, $V_L=0V$ (same as for inverter!)

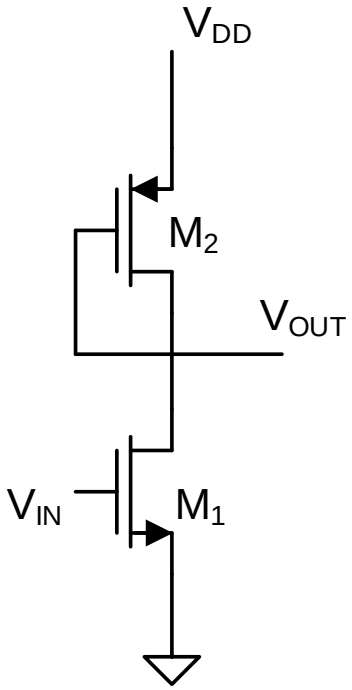


Arbitrary PUN and PDN

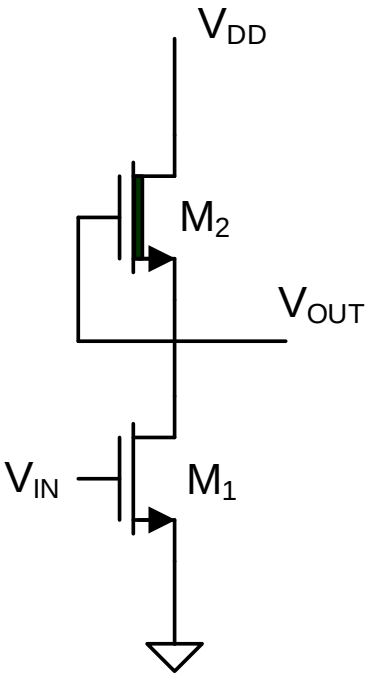
Other MOS Logic Families



Enhancement Load
NMOS

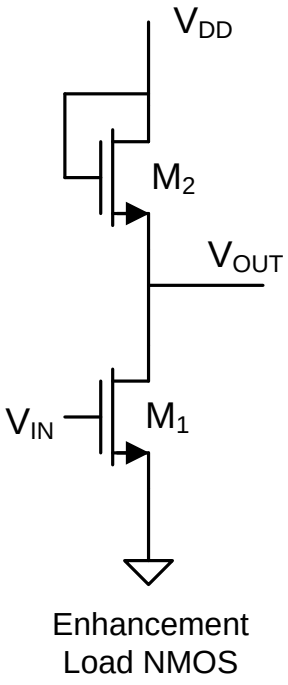


Enhancement Load
Pseudo-NMOS

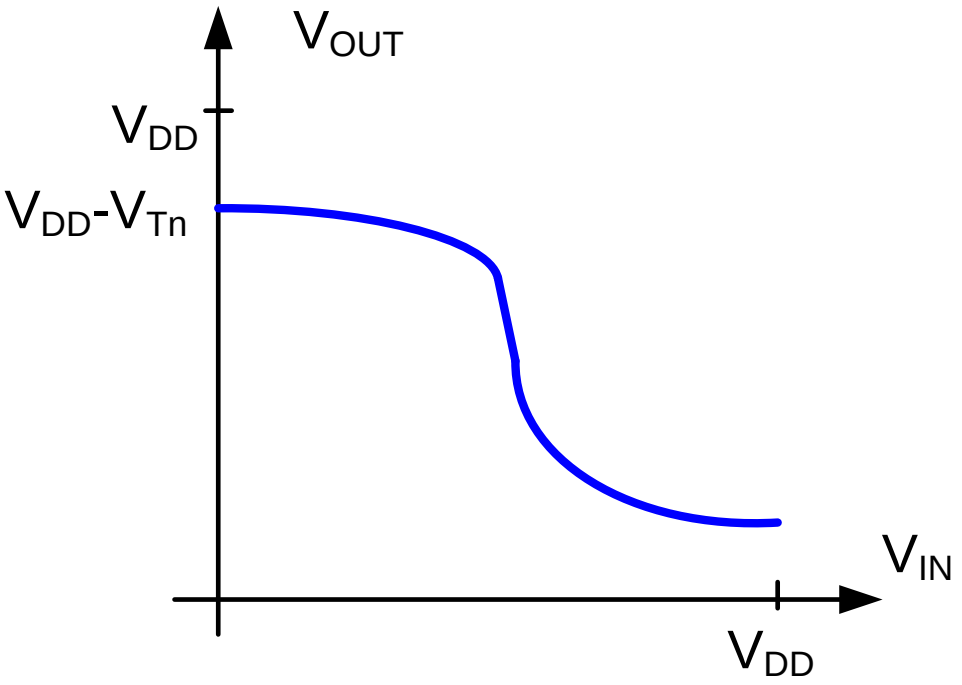


Depletion Load
NMOS

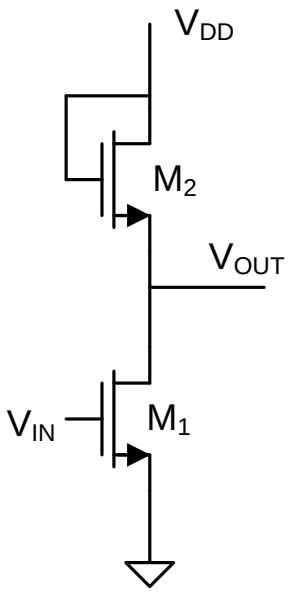
Other CMOS/MOS Logic Families



Enhancement
Load NMOS

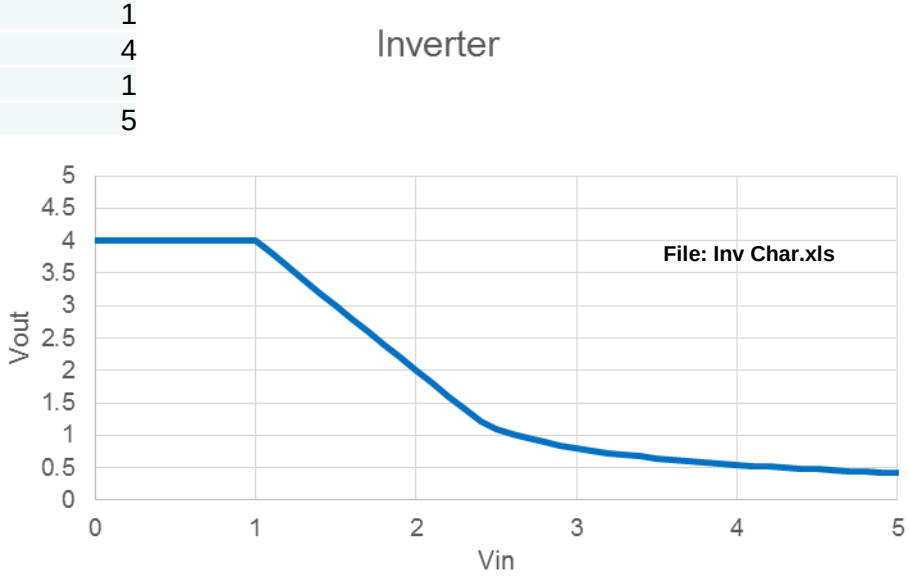


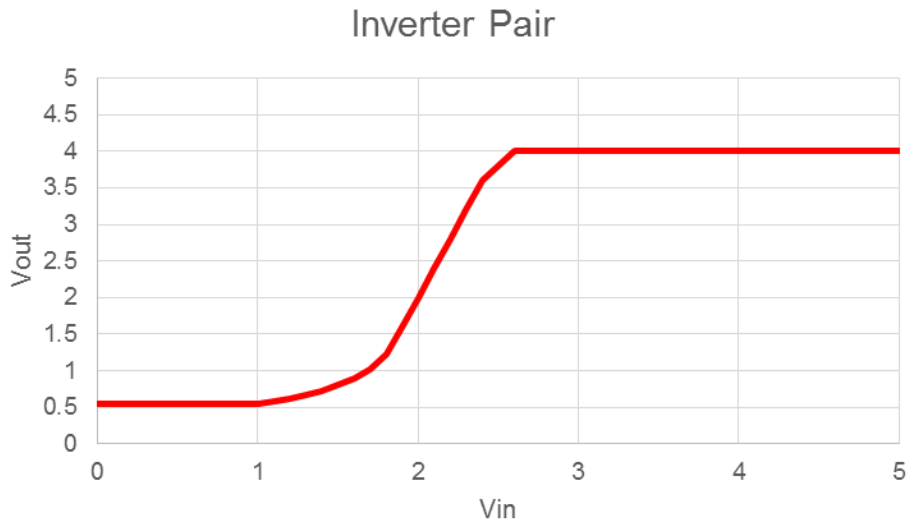
NMOS example



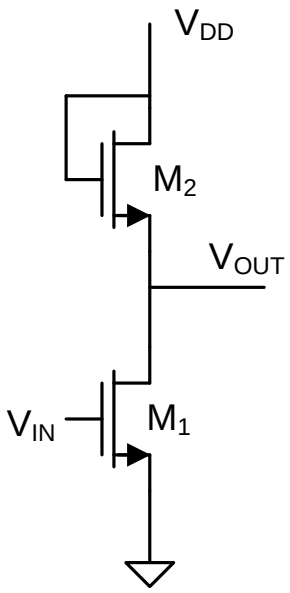
Enhancement
Load NMOS

VTH	1
W1/L1	4
W2/L2	1
VDD	5





NMOS example



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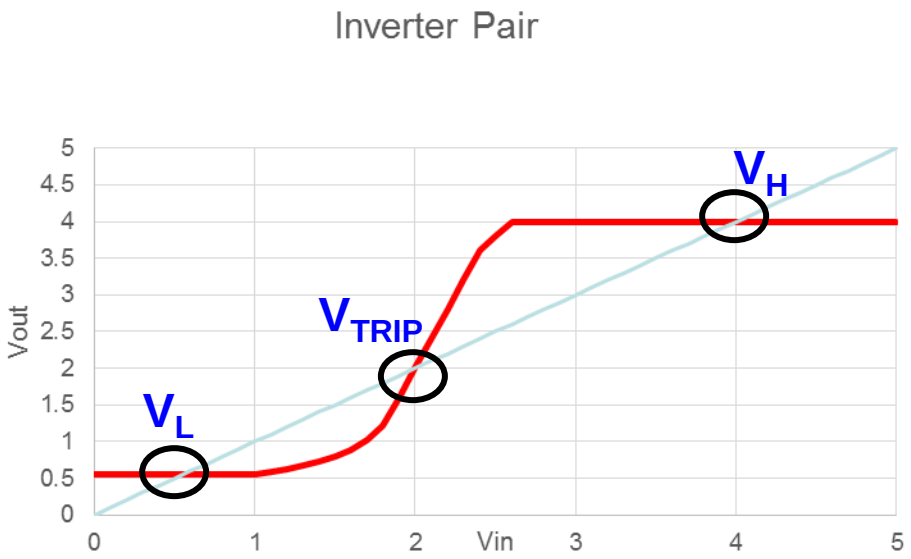
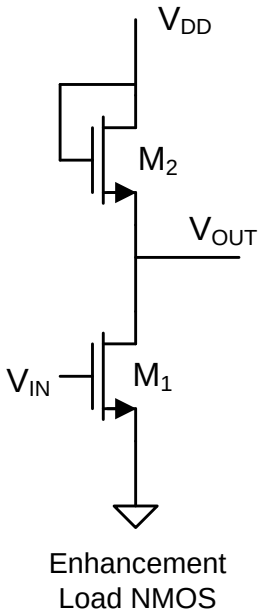
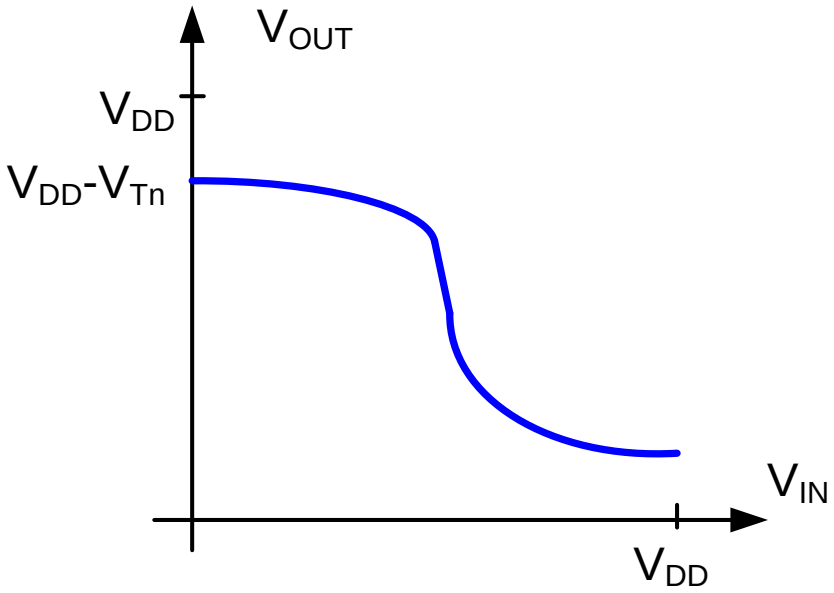


V_H=4V
V_L=0.55V
V_{TRIP}=2V

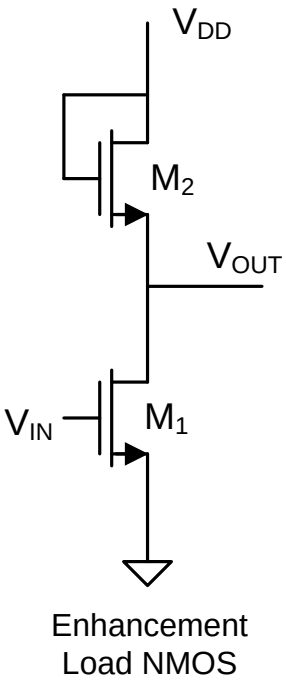
Other CMOS/MOS Logic Families



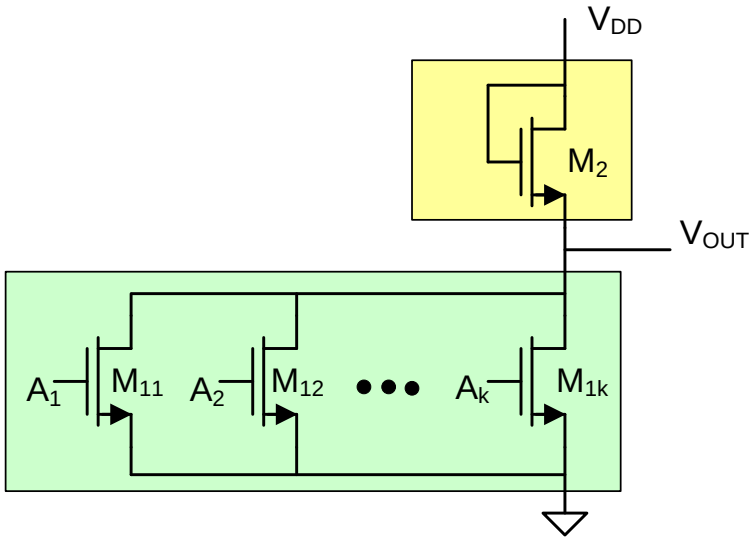


- **High and low swings are reduced**
- **Response time is slow on LH output transitions**
- **Static Power Dissipation Large when V_{OUT} is low (will sl**
- **Very economical process**
- **Termed "ratio logic" (because logic values dependent on device W/L ratios – USE UP DOF!)**
- **May not work for some device sizes**
- **Compact layout (no wells !)**
- **Can use very low cost process**
- **Available to use in standard CMOS process**

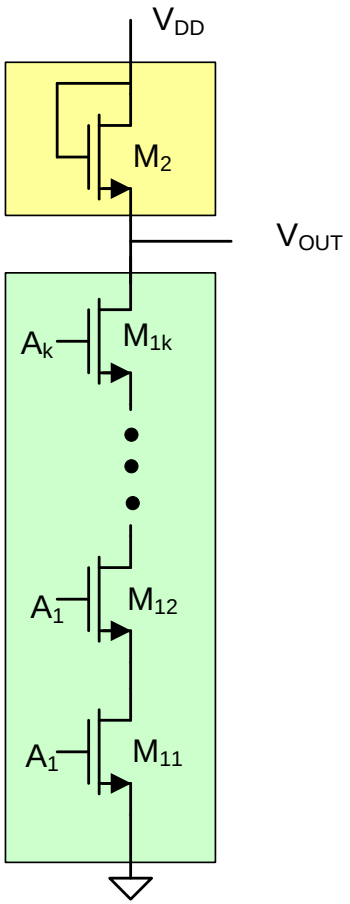
Other CMOS/MOS Logic Families



Enhancement Load NMOS



k-input NOR



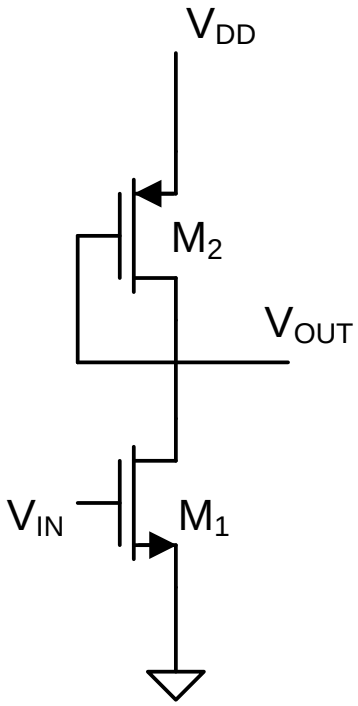
k-input NAND

- **Multiple-input gates require single transistor for each additional input**

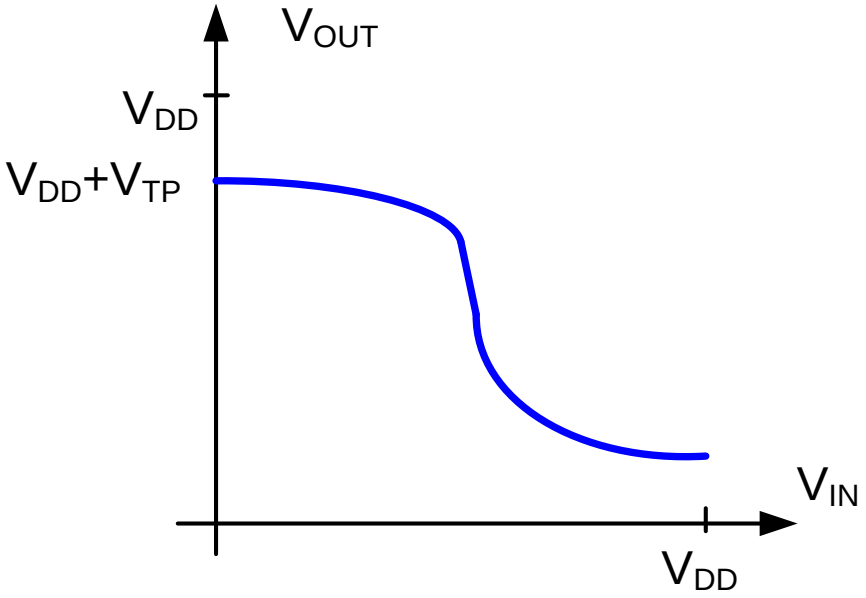
- **Still useful if many inputs are required**

(will be shown that static power does not increase with k)

Other CMOS/MOS Logic Families

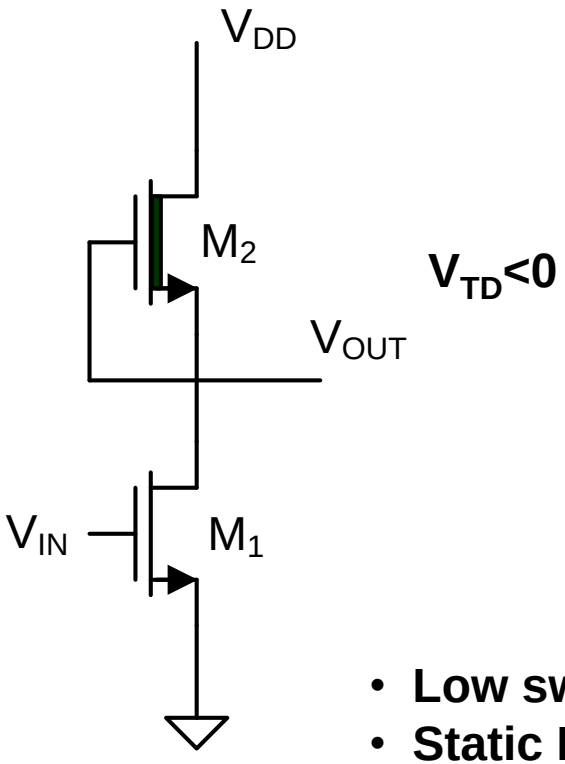


Enhancement Load
Pseudo-NMOS



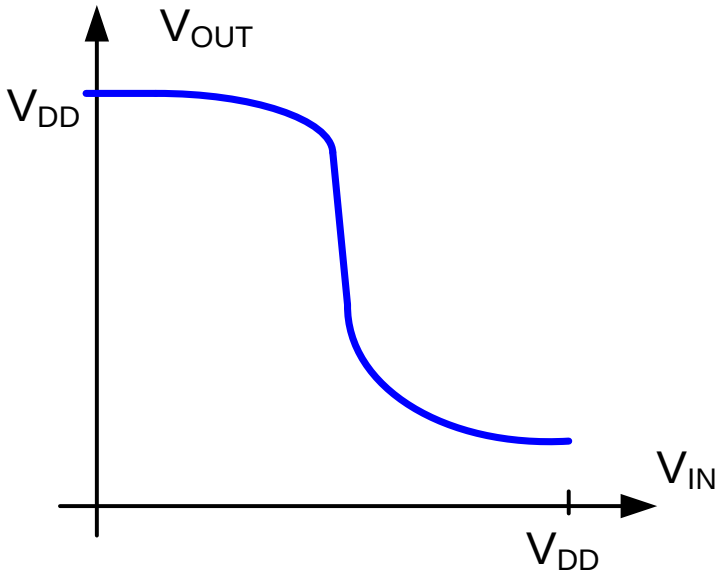
- **High and low swings are reduced**
- **Response time is slow on LH output transitions**
- **Static Power Dissipation Large when V_{OUT} is low**
- **Multiple-input gates require single transistor for each additional input**
- **Termed “ratio” logic**
- **Available to use in standard CMOS process**

Other CMOS/MOS Logic Families



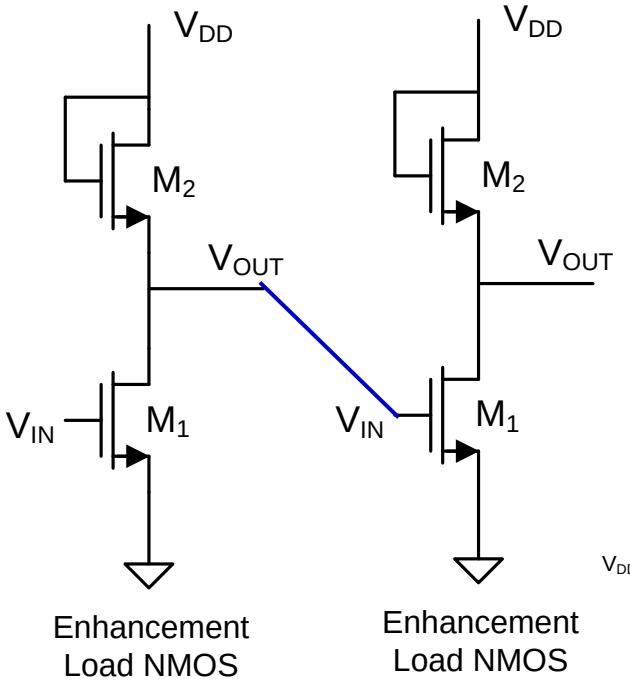
Depletion Load NMOS

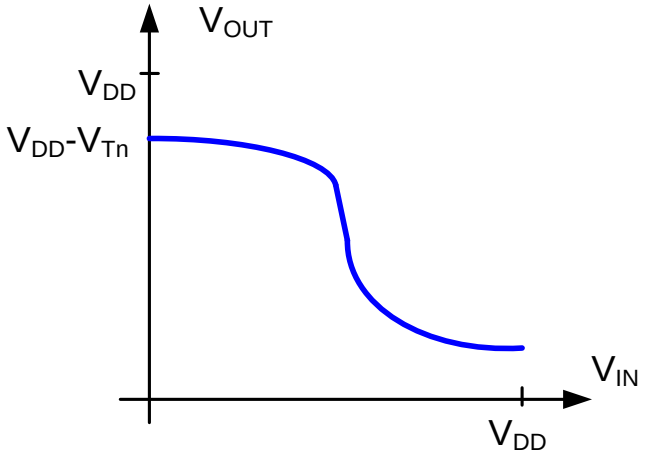
$V_{TD}<0$

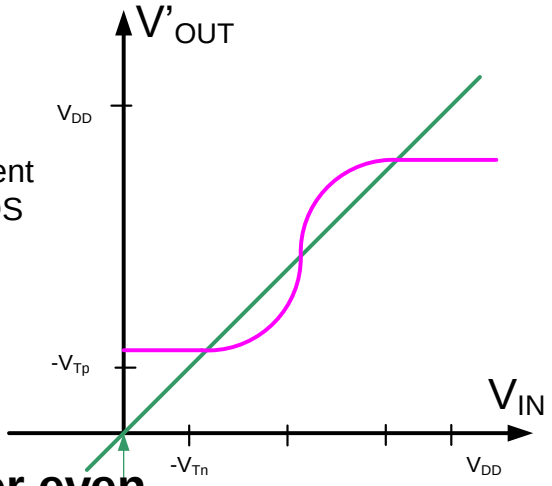


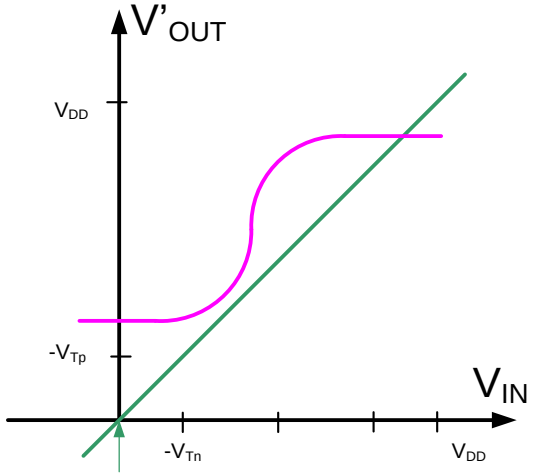
- **Low swing is degraded**
- **Static Power Dissipation Large when V_{OUT} is low**
- **Very economical process**
- **Better than Enhancement Load NMOS**
- **Termed “ratio” logic**
- **Compact layout (no wells !)**
- **Response time slow on L-H output transitions**
- **Dominant MOS logic until about 1985**
- **Depletion device not available in most processes today**

Other CMOS/MOS Logic Families



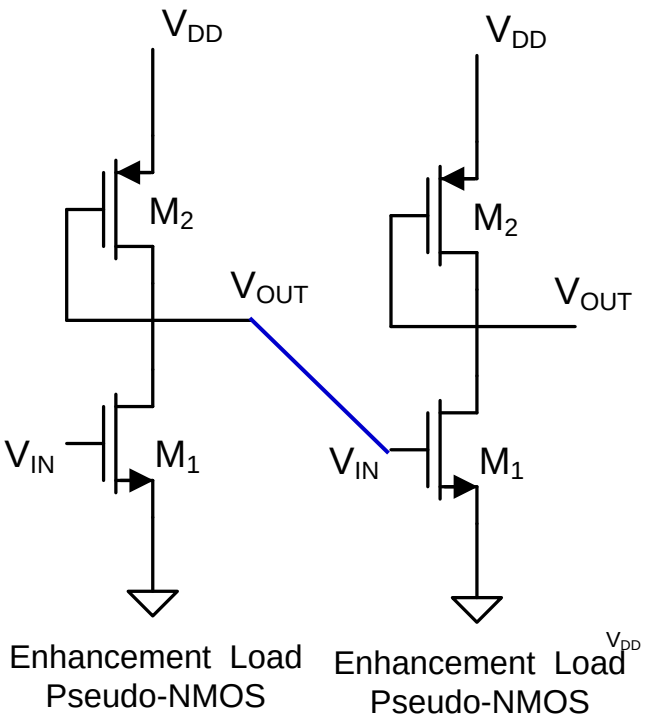






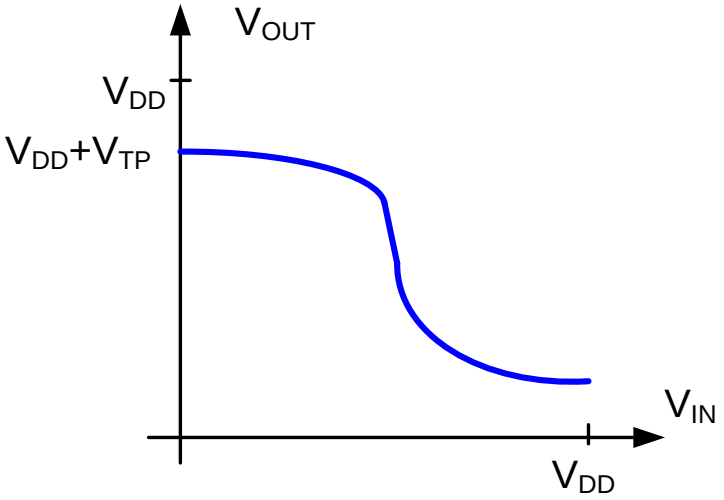
- **Reduced V_H-V_L**
- **Device sizing critical for even basic operation**
- **Shallow slope at V_{TRIP}**

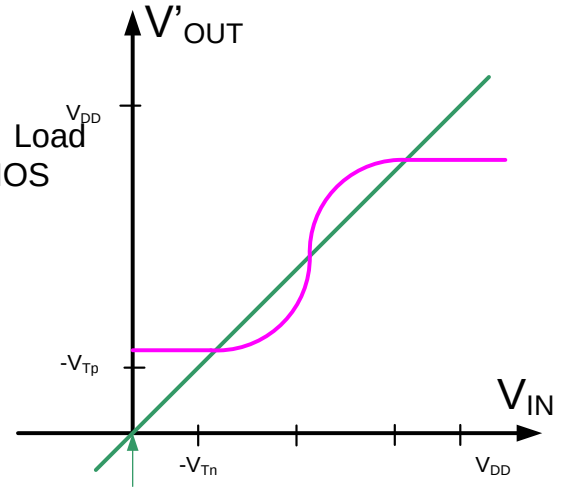
Other CMOS/MOS Logic Families

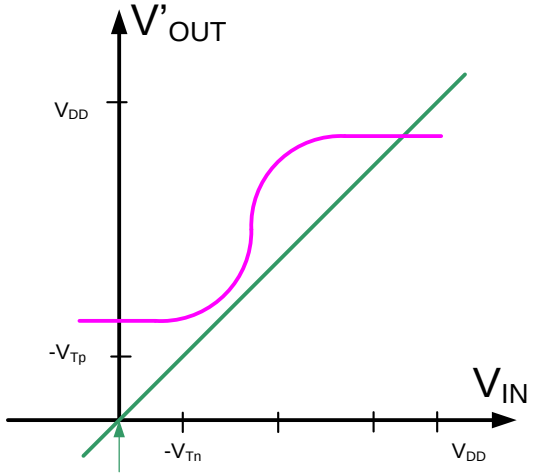


Enhancement Load Pseudo-NMOS

Enhancement Load Pseudo-NMOS

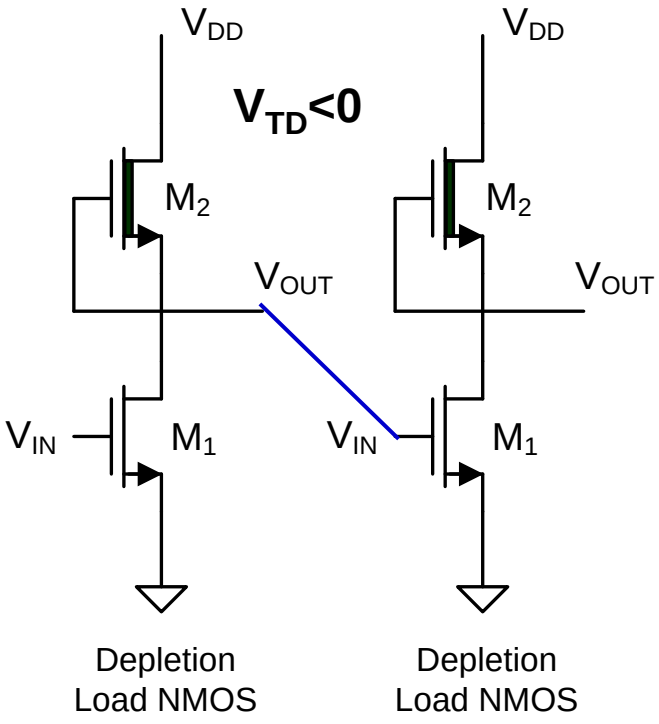


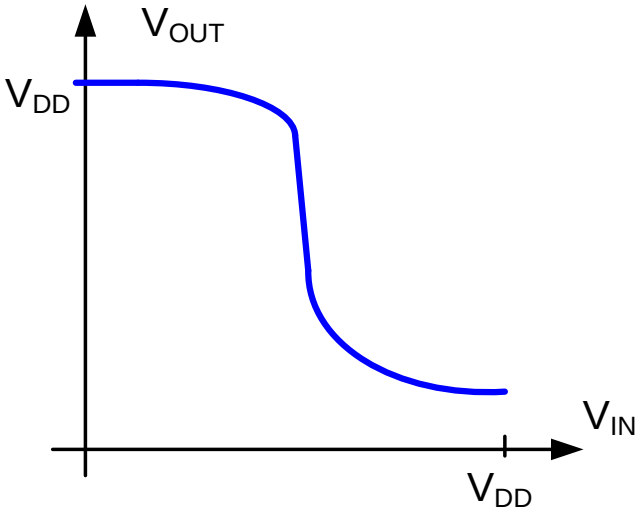


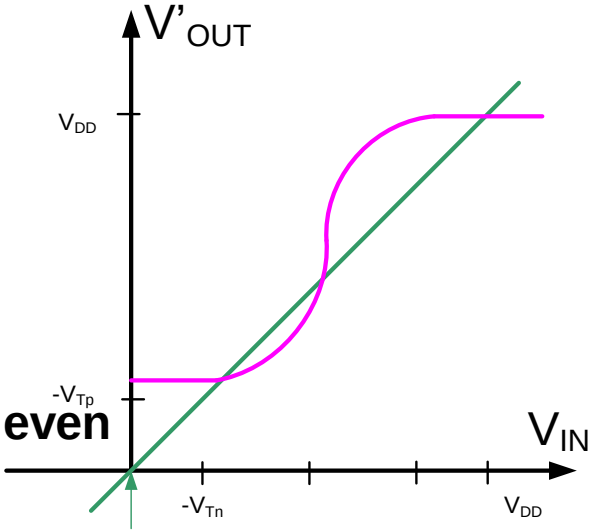


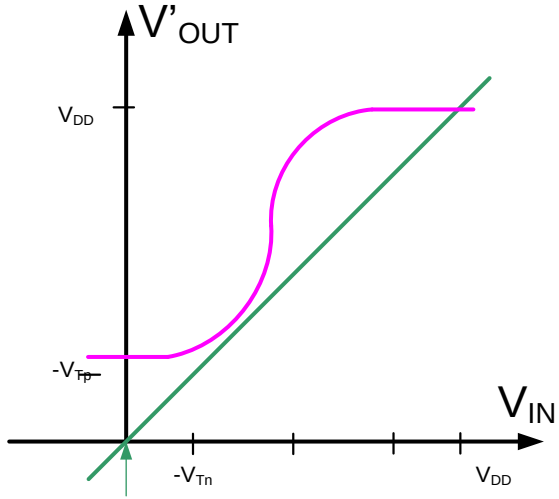
- **Reduced V_H-V_L**
- **Device sizing critical for even basic operation (DOF)**
- **Shallow slope at V_{TRIP}**

Other CMOS/MOS Logic Families









- **Reduced V_H-V_L**
- **Device sizing critical for even basic operation**
- **Shallow slope at V_{TRIP}**

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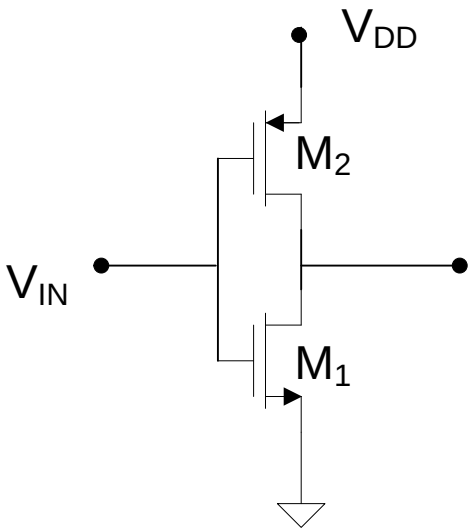
done

partial

Static Power Dissipation in Static CMOS Family

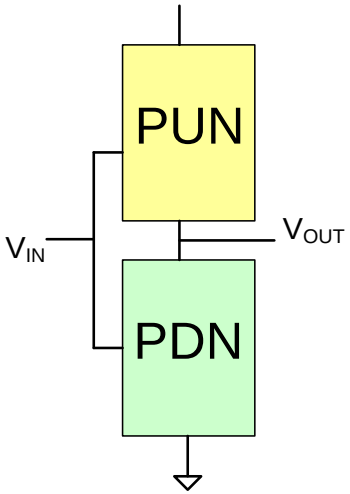


When V_{IN} is Low and V_{OUT} is High, M_1 is off and I_{D1}=0

When V_{IN} is High and V_{OUT} is Low, M_2 is off and I_{D2}=0

Thus, P_{STATIC}=0

This is a key property of the static CMOS Logic Family ➔the major reason Static CMOS Logic is so dominant

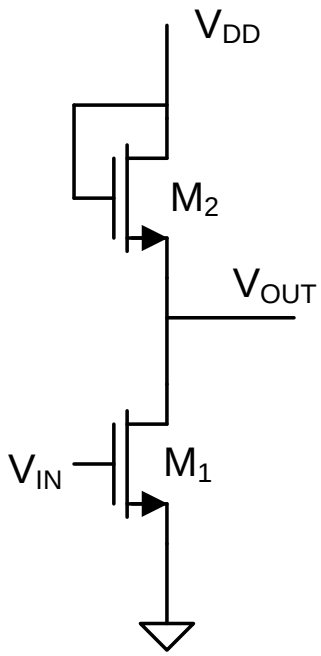


It can be shown that this zero static power dissipation property can be preserved if the PUN is comprised of p-channel devices, the PDN is comprised of n-channel devices and they are never both driven into the conducting states at the same time

Compound Gate in CMOS Process

Static Power Dissipation in Ratio Logic Families

Example:



Enhancement Load NMOS

Assume V_{DD}=5V
V_T=1V, μC_{OX} =10^{-4}A/V^2, W_1/L_1=1 and M_2 sized so that V_L is close to V_{Tn}

Observe:

$V_H=V_{DD}-V_{Tn}$

If $V_{IN}=V_H$, $V_{OUT}=V_L$ so

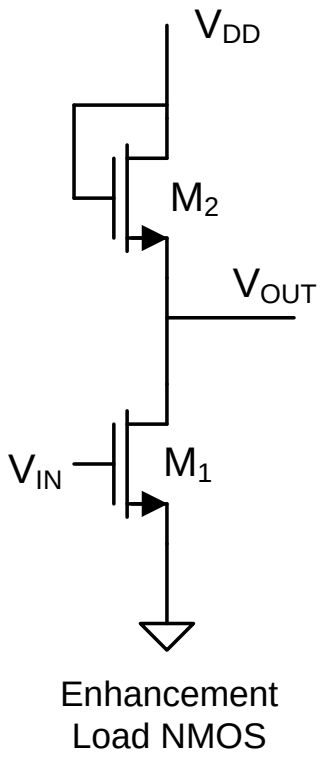
$$I_{D1} = \frac{\mu C_{OX} W_1}{L_1}\left(V_{GS1} - V_T - \frac{V_{DS1}}{2}\right)V_{DS1}$$

$$I_{D1} = 10^{-4}\left(5 - 1 - 1 - \frac{1}{2}\right)\bullet 1 = 0.25\text{mA}$$

P_L=(5V)(0.25mA)=1.25mW

Static Power Dissipation in Ratio Logic Families

Example:



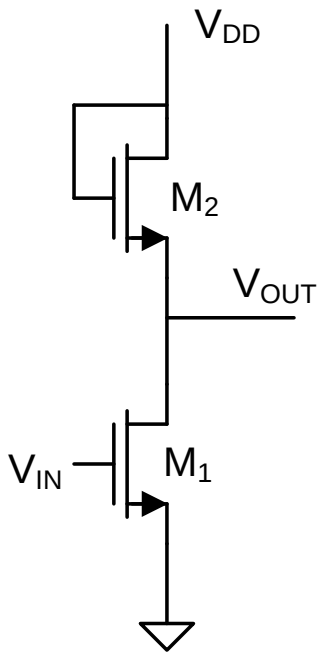
Assume V_{DD}=5V
V_T=1V, μC_{OX} =10^{-4}A/V^2, W_1/L_1=1 and M_2 sized so that V_L is close to V_{Tn}

P_L=(5V)(0.25mA)=1.25mW

If a circuit has 100,000 gates and half of them are in the V_{OUT}=V_L state, the static power dissipation will be

Static Power Dissipation in Ratio Logic Families

Example:



Enhancement Load NMOS

Assume V_{DD}=5V
V_T=1V, μC_{OX} =10^{-4}A/V^2, W_1/L_1=1 and M_2 sized so that V_L is close to V_{Tn}

P_L=(5V)(0.25mA)=1.25mW

If a circuit has 100,000 gates and half of them are in the V_{OUT}=V_L state, the static power dissipation will be

$$P_{STATIC} = \frac{1}{2}10^5 \bullet 1.25mW = \mathbf{62.5W}$$

This power dissipation is way too high and would be even larger in circuits with 100 million or more gates – the level of integration common in SoC circuits today

Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
    - FI/OD
    - Logical Effort
  - Elmore Delay
- Sizing of Gates
  - The Reference Inverter

- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators

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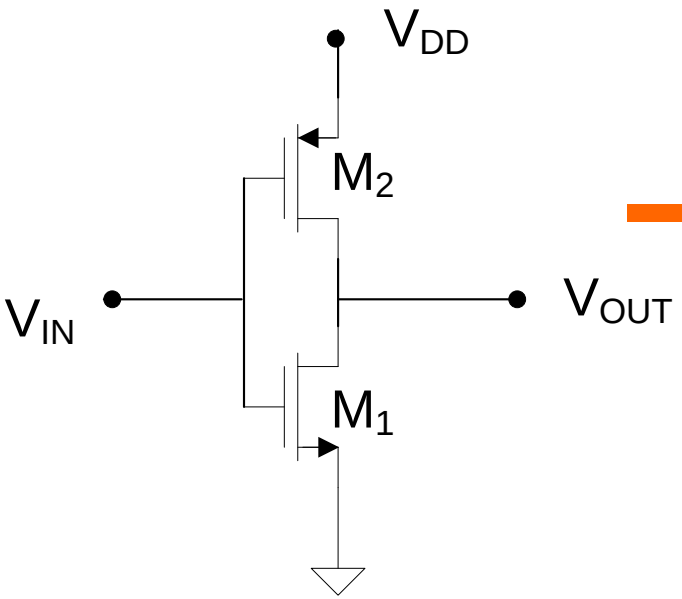
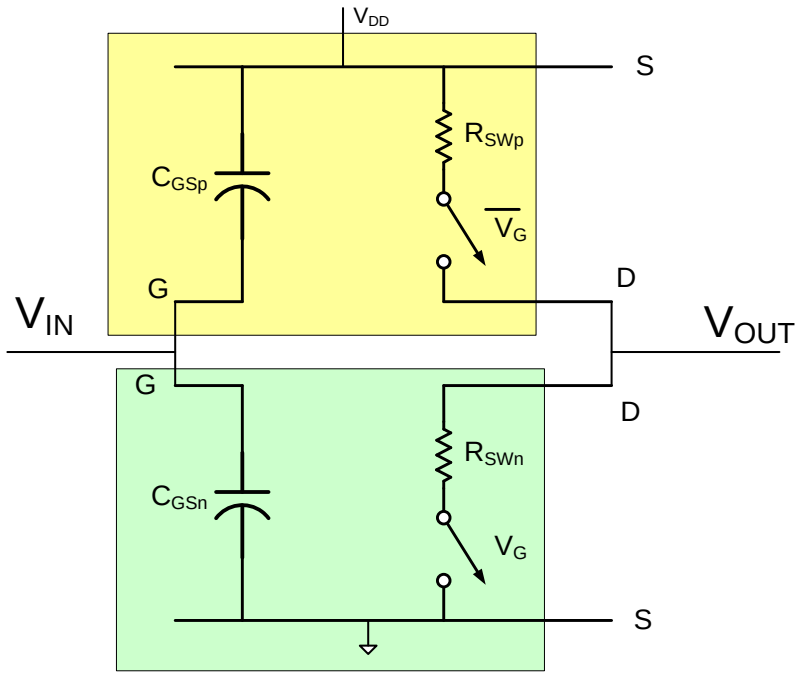
done

partial

Propagation Delay in Static CMOS Family

(Review from earlier discussions)

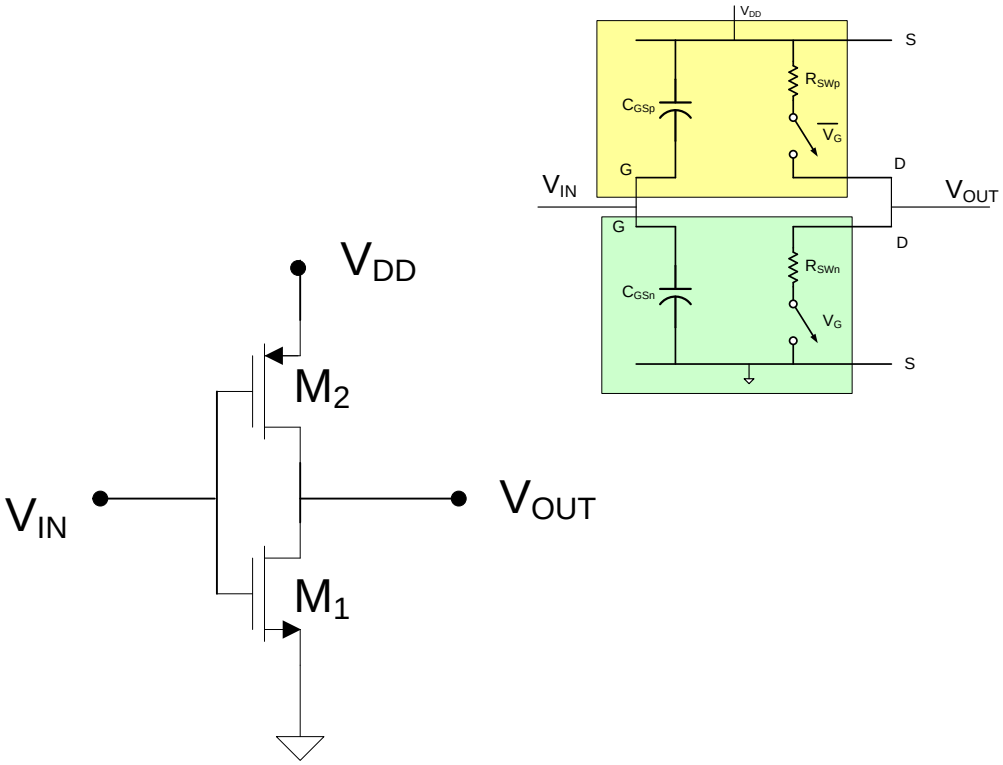


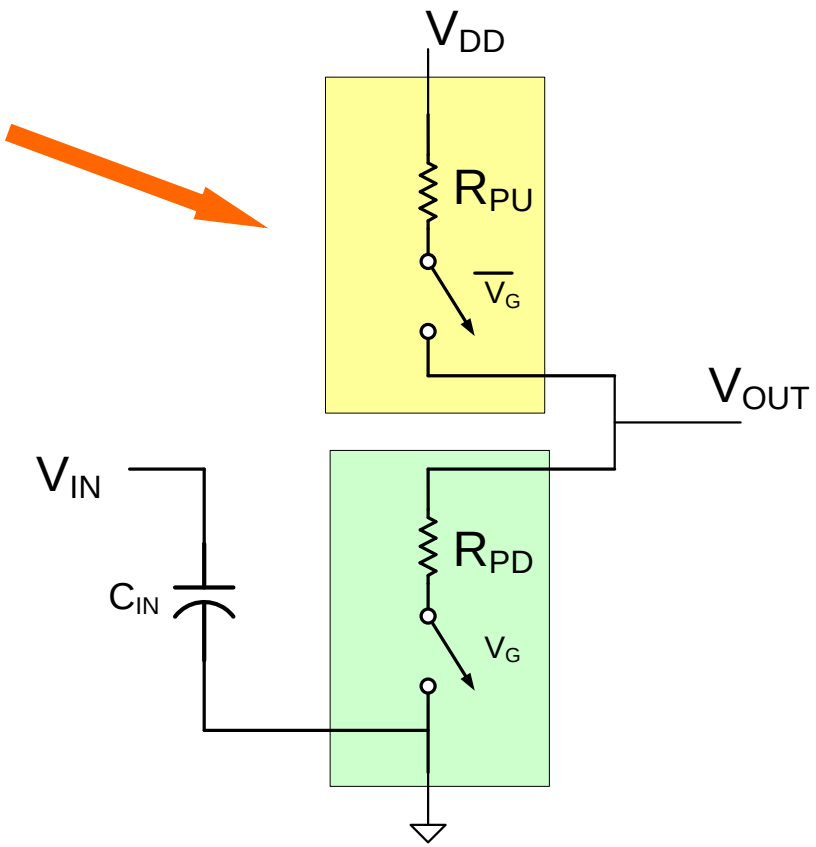


Switch-level model of Static CMOS inverter (neglecting diffusion parasitics)

Propagation Delay in Static CMOS Family

(Review from earlier discussions)

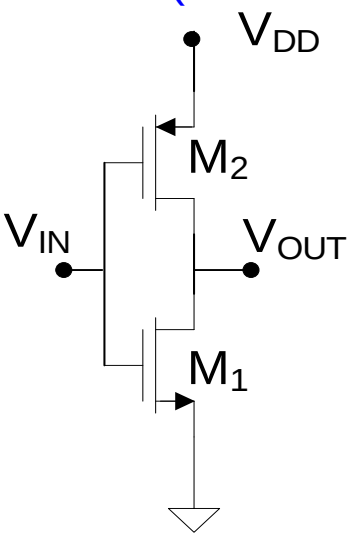


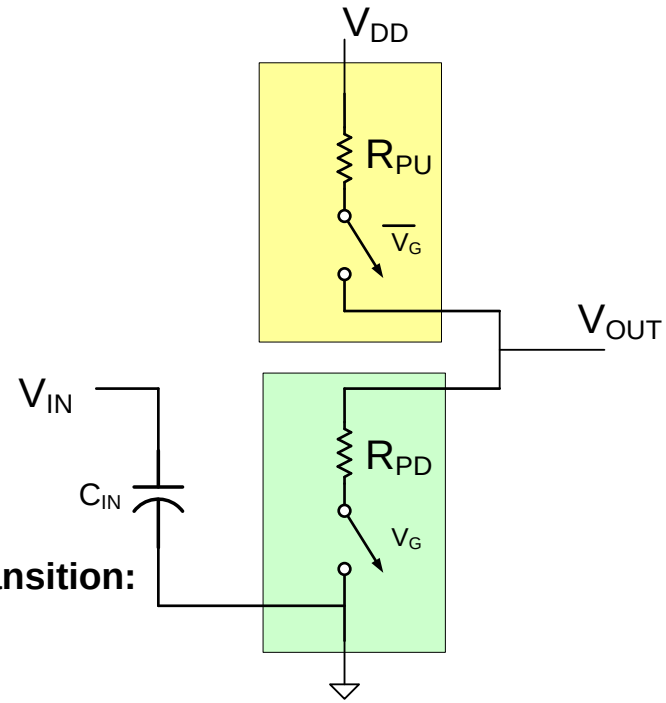


Switch-level model of Static CMOS inverter (neglecting diffusion parasitics)

Propagation Delay in Static CMOS Family

(Review from earlier discussions)





Since conducting transistor operating in triode through most of transition:

$$I_D \cong \frac{\mu C_{OX} W}{L}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} \cong \frac{\mu C_{OX} W}{L}\left(V_{GS} - V_T\right)V_{DS}$$

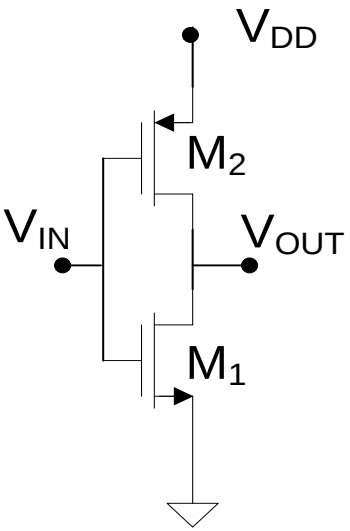
$$R_{PD} = \frac{V_{DS}}{I_D} = \frac{L_1}{\mu_n C_{OX} W_1 \left(V_{DD} - V_{Tn}\right)}$$

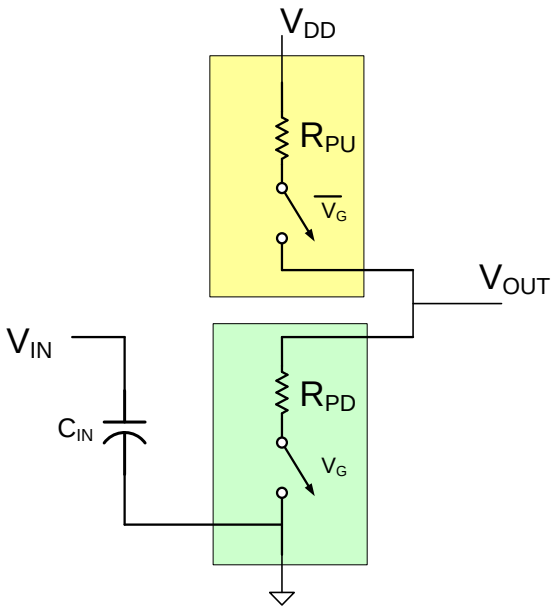
$$R_{PU} = \frac{V_{DS}}{I_D} = \frac{L_2}{\mu_p C_{OX} W_2 \left(V_{DD} + V_{Tp}\right)}$$

$$C_{IN} = C_{OX}\left(W_1 L_1 + W_2 L_2\right)$$

Propagation Delay in Static CMOS Family

(Review from earlier discussions)





$$R_{PD} = \frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_{Tn})}$$

$$R_{PU} = \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} + V_{Tp})}$$

$$C_{IN} = C_{OX}(W_1 L_1 + W_2 L_2)$$

Example: Minimum-sized M_1 and M_2

If $u_n C_{OX}$=100μAV^{-2}, C_{OX}=4 fFμ^{-2} , $V_{Tn}=V_{DD}/5$, $V_{TP}=-V_{DD}/5$, $\mu_n/\mu_p=3$, $L_1=W_1=L_{MIN}$, $L_2=W_2=L_{MIN}$, L_{MIN}=0.5μ and V_{DD}=5V

(Note: This C_{OX} is somewhat larger than that in the 0.5u ON process)

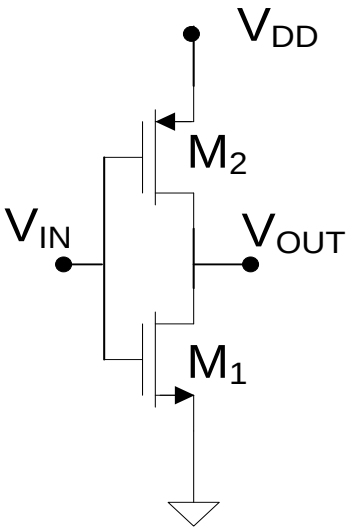
$$R_{PD} = \frac{1}{10^{-4} \bullet 0.8V_{DD}} = 2.5K\Omega$$

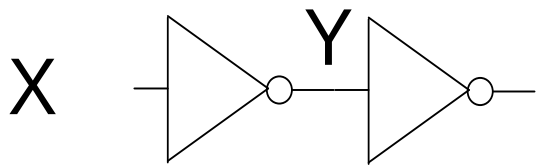
$$R_{PU} = \frac{1}{10^{-4} \bullet \frac{1}{3} \bullet 0.8V_{DD}} = 7.5K\Omega$$

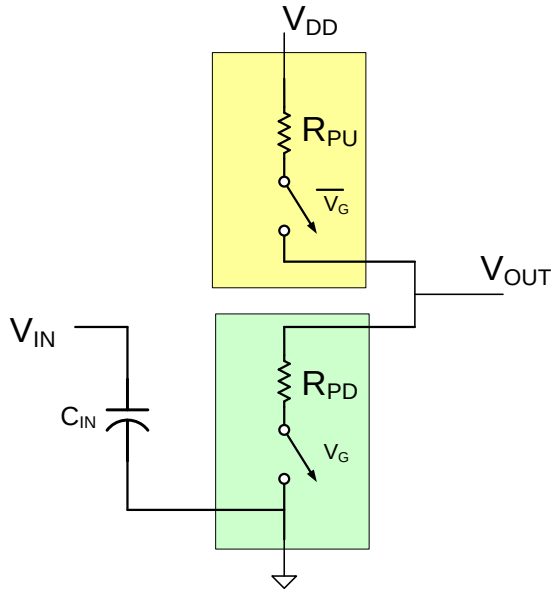
$$C_{IN} = 4 \bullet 10^{-15} \bullet 2L_{MIN}^2 = 2fF$$

Propagation Delay in Static CMOS Family

(Review from earlier discussions)







In typical process with Minimum-sized M_1 and M_2 :

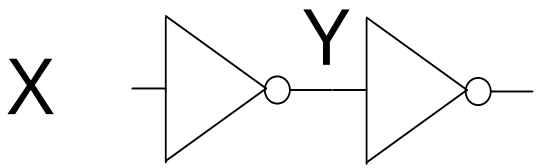
$$R_{PD} \cong 2.5K\Omega$$

$$R_{PU} \cong 3R_{PD} = 7.5K\Omega$$

$$C_{IN} \cong 2fF$$

Propagation Delay in Static CMOS Family

(Review from earlier discussions)



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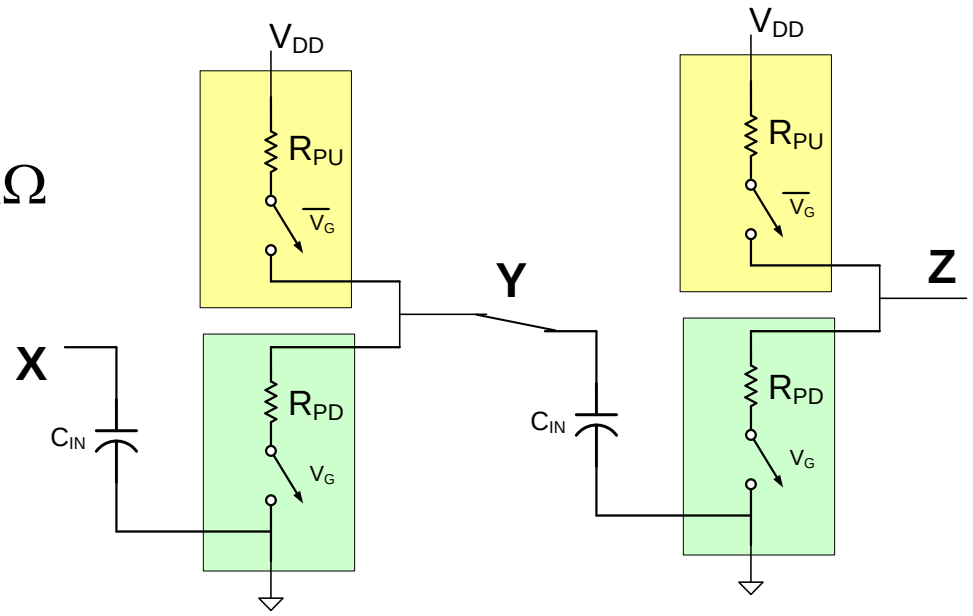
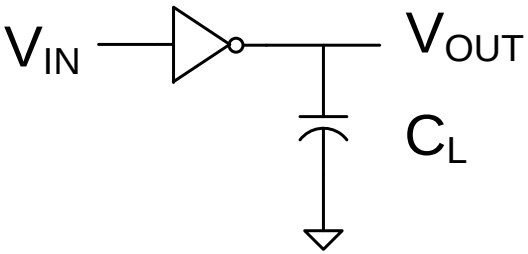


How long does it take for a signal to propagate from x to y?

Propagation Delay in Static CMOS Family

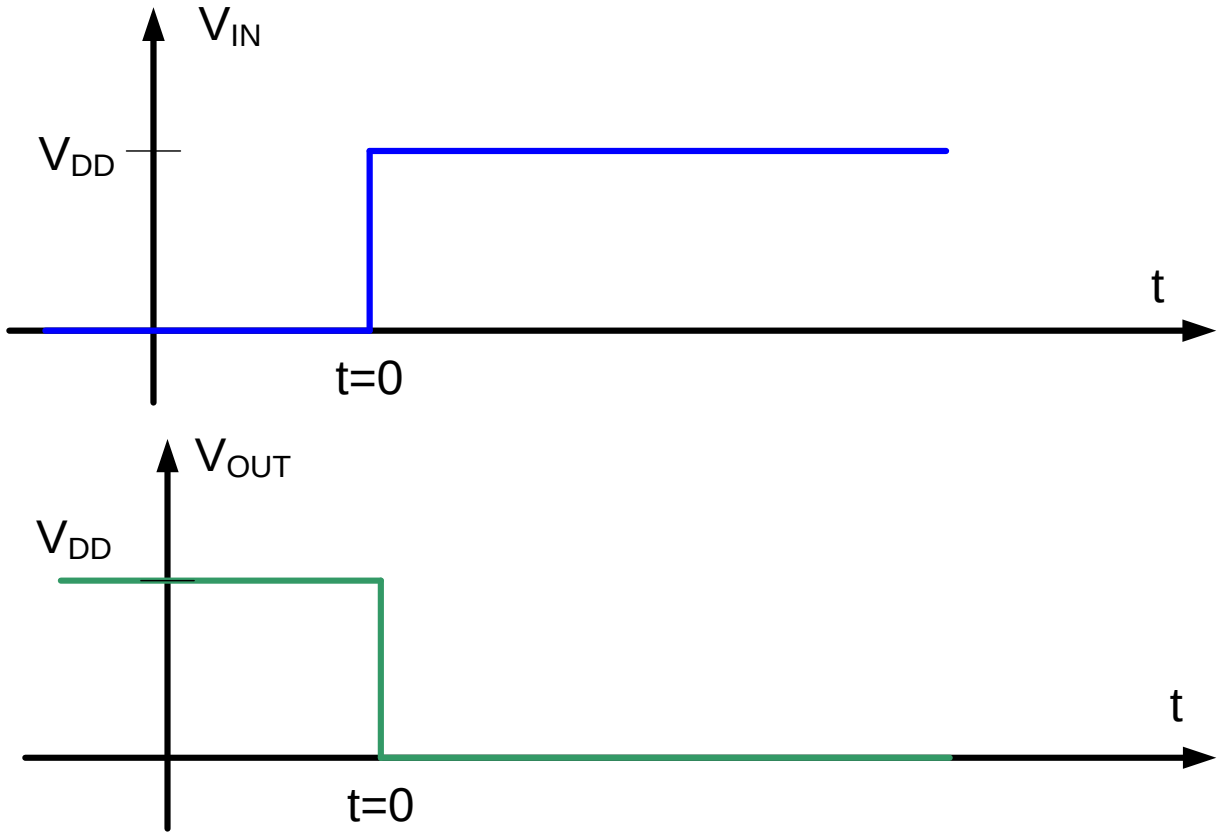
(Review from earlier discussions)

Consider:



For HL output transition, C_L charged to V_{DD}

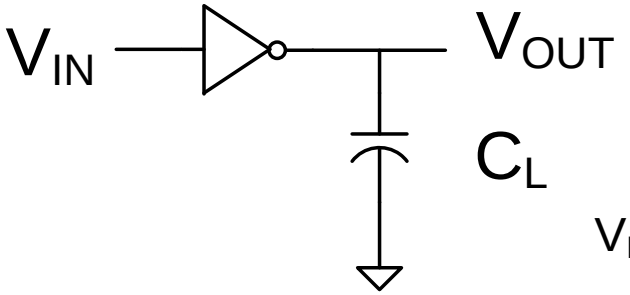
Ideally:



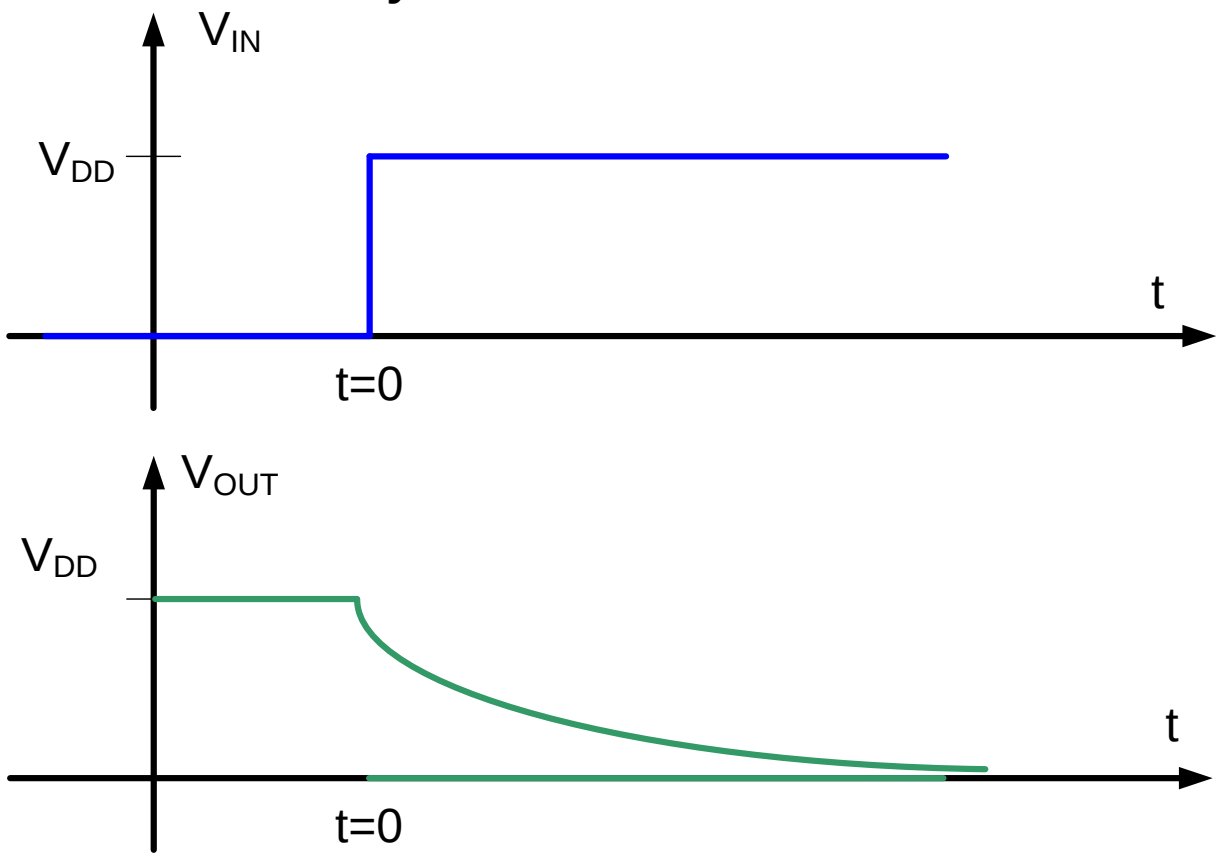
Propagation Delay in Static CMOS Family

(Review from earlier discussions)

For HL output transition, C_L charged to V_{DD}



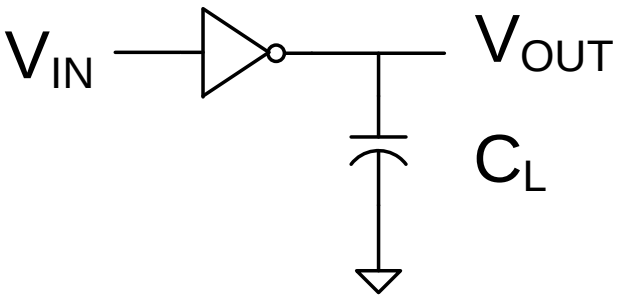
Actually:

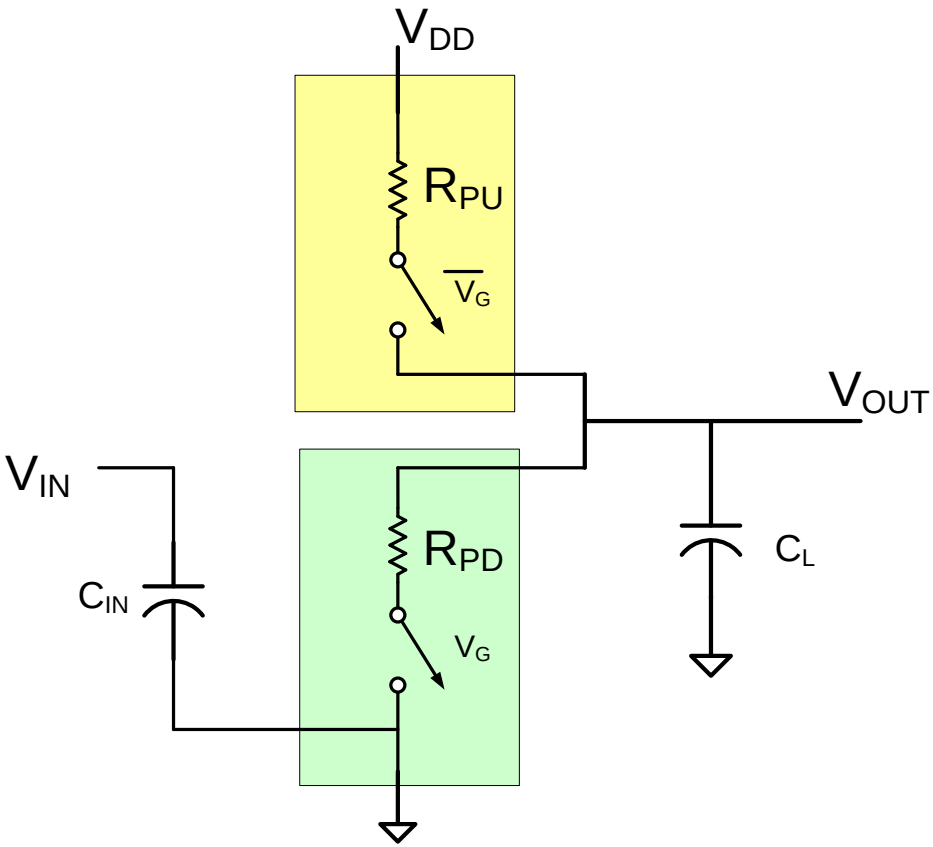


What is the transition time t_{HL} ?

Propagation Delay in Static CMOS Family

(Review from earlier discussions)

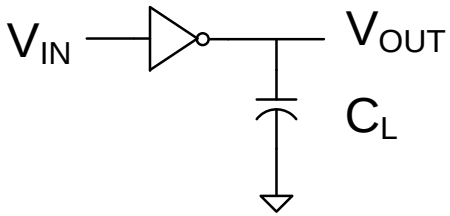


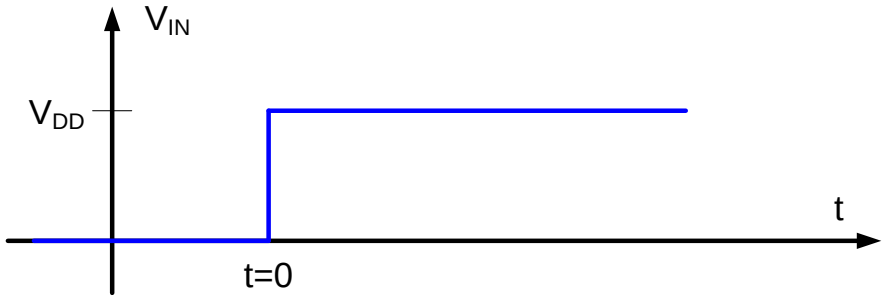


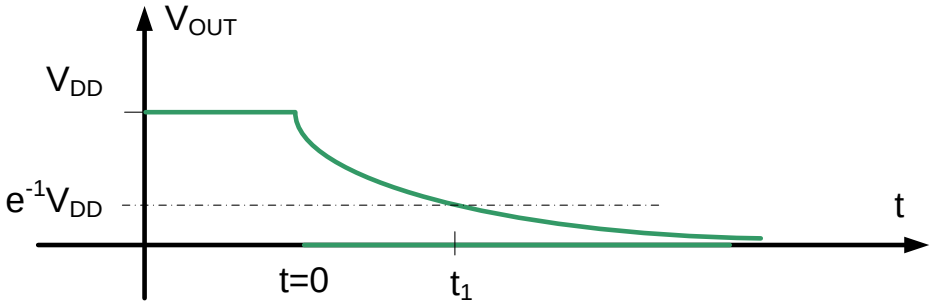
Propagation Delay in Static CMOS Family

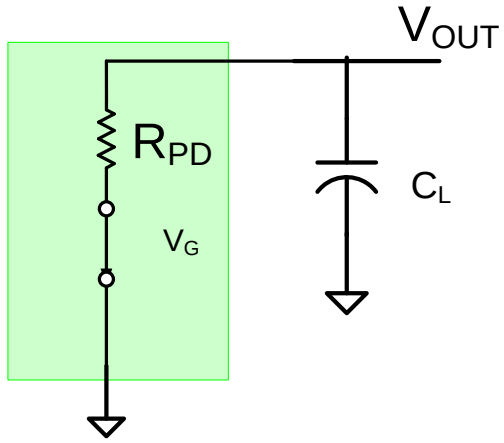
(Review from earlier discussions)

For HL output transition, C_L charged to V_{DD}









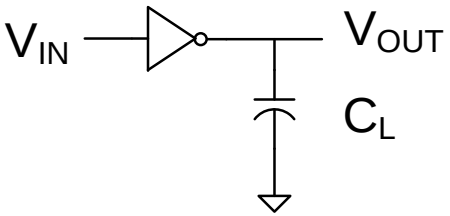
$$V_{OUT}(t) = F + (I - F)e^{\frac{-t}{\tau}} = 0 + (V_{DD} - 0)e^{-\frac{t}{R_{PD}C_L}}$$

$$\frac{V_{DD}}{e} = V_{DD}e^{-\frac{t_1}{R_{PD}C_L}} \quad \Rightarrow \quad t_1 = R_{PD}C_L$$

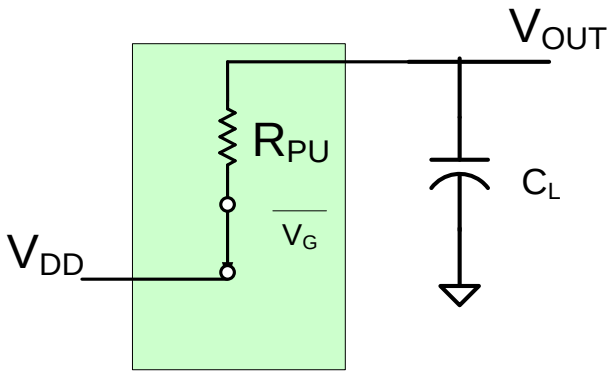
If V_{TRIP} is close to $V_{DD}/2$, t_{HL} is close to t_1

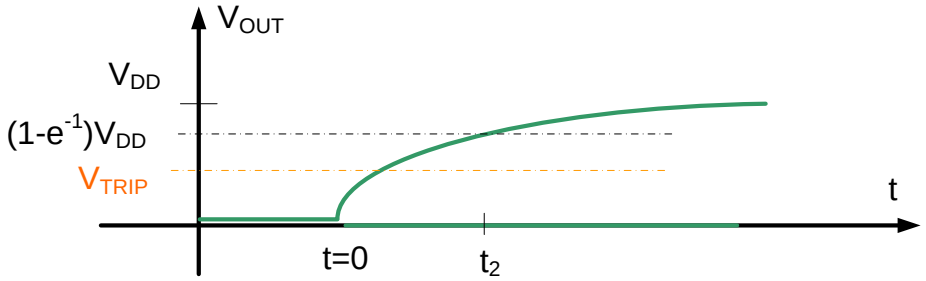
Propagation Delay in Static CMOS Family

(Review from earlier discussions)



For HL output transition, C_L charged to V_{DD}





$$t_{LH} \cong t_2 = R_{PU}C_L$$

Summary:

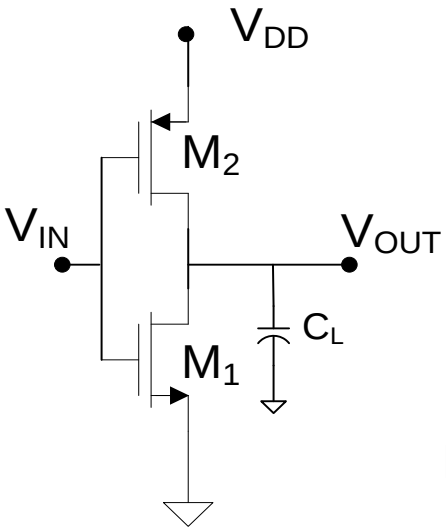
$$t_{LH} \cong R_{PU}C_L$$

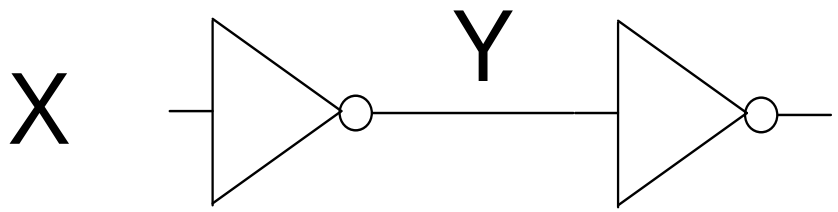
$$t_{HL} \cong R_{PD}C_L$$

For V_{TRIP} close to $V_{DD}/2$

Propagation Delay in Static CMOS Family

(Review from earlier discussions)





In typical process with Minimum-sized M_1 and M_2 :

$$t_{HL} \cong R_{PD}C_L \cong 2.5K \bullet 2fF = 5ps$$

$$t_{LH} \cong R_{PU}C_L \cong 7.5K \bullet 2fF = 15ps$$

(Note: This C_{ox} is somewhat larger than that in the 0.5u ON process)

Note: LH transition is much slower than HL transition

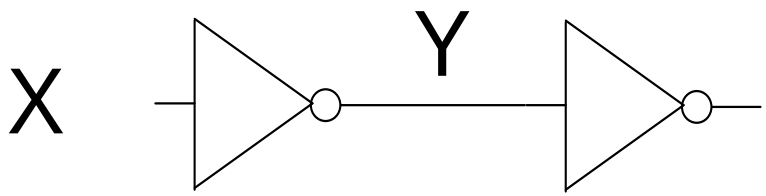
Propagation Delay in Static CMOS Family

Defn: The Propagation Delay of a gate is defined to be the sum of t_{HL} and t_{LH}, that is, $t_{PROP}=t_{HL}+t_{LH}$

$$t_{PROP} = t_{HL} + t_{LH} \cong C_L \left(R_{PU} + R_{PD}\right)$$

Propagation delay represents a fundamental limit on the speed a gate can be clocked at

For basic two-inverter cascade in static 0.5um CMOS logic



$$t_{PROP} = t_{HL} + t_{LH} \cong 20\,p\,\text{sec}$$

Propagation Delay in Static CMOS Family

$$t_{PROP} = t_{HL} + t_{LH} \cong C_L\left(R_{PU} + R_{PD}\right)$$

$$R_{PD} = \frac{L_1}{\mu_n C_{OX} W_1 \left(V_{DD} - V_{Tn}\right)} \qquad R_{PU} = \frac{L_2}{\mu_p C_{OX} W_2 \left(V_{DD} + V_{Tp}\right)} \qquad C_{IN} = C_{OX}\left(W_1 L_1 + W_2 L_2\right)$$

If $V_{Tn} = -V_{Tp} = V_T$

$$t_{PROP} = C_{OX}\left(W_1 L_1 + W_2 L_2\right)\left(\frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_T)} + \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} - V_T)}\right)$$

If $L_2 = L_1 = L_{\min}$, $\mu_n = 3\mu_p$,

$$t_{PROP} = \frac{L_{\min}^2}{\mu_n (V_{DD} - V_T)}(W_1 + W_2)\left(\frac{1}{W_1} + \frac{3}{W_2}\right) = \frac{L_{\min}^2}{\mu_n (V_{DD} - V_T)}\left(4 + \frac{W_2}{W_1} + 3\frac{W_1}{W_2}\right)$$

Note speed is s function of device sizing !

Can t_{PROP} be minimized?

Propagation Delay in Static CMOS Family

For $L_2 = L_1 = L_{\min},\ \mu_n = 3\mu_p,$

$$t_{PROP} = \frac{L_{\min}^2}{\mu_n (V_{DD} - V_T)} \left(4 + \frac{W_2}{W_1} + 3\frac{W_1}{W_2}\right)$$

Can t_{PROP} be minimized?

Assume $W_1 = W_{MIN}$

$$\frac{\partial t_{PROP}}{\partial W_2} = \left[\frac{L_{min}^2}{\mu_n \left(V_{DD} - V_{TH}\right)}\right]\left[\frac{1}{W_{MIN}} - 3\frac{W_{MIN}}{W_2^2}\right] = 0$$

$$\frac{1}{W_{MIN}} - 3\frac{W_{MIN}}{W_2^2} = 0$$

$$W_2 = \sqrt{3} W_{MIN}$$

$$t_{PROP} = \frac{L_{\min}^2}{\mu_n (V_{DD} - V_T)} (4 + 2\sqrt{3}) \cong \frac{L_{\min}^2}{\mu_n (V_{DD} - V_T)} (7.5)$$

Propagation Delay in Static CMOS Family

$$t_{PROP} = t_{HL} + t_{LH} \cong C_L\left(R_{PU} + R_{PD}\right)$$

$$R_{PD} = \frac{L_1}{\mu_n C_{OX} W_1 \left(V_{DD} - V_{Tn}\right)} \qquad R_{PU} = \frac{L_2}{\mu_p C_{OX} W_2 \left(V_{DD} + V_{Tp}\right)} \qquad C_{IN} = C_{OX}\left(W_1 L_1 + W_2 L_2\right)$$

If $V_{Tn} = -V_{Tp} = V_T$

$$t_{PROP} = C_{OX}(W_1 L_1 + W_2 L_2)\left(\frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_T)} + \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} - V_T)}\right)$$

If $L_2 = L_1 = L_{min}$, $\mu_n = 3\mu_p$,

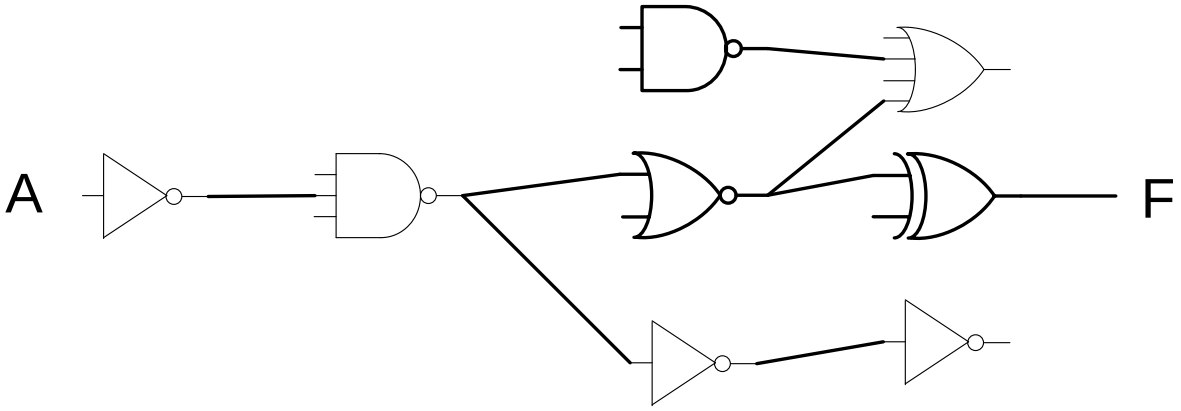
$$t_{PROP} = \frac{L_{min}^2}{\mu_n (V_{DD} - V_T)}(W_1 + W_2)\left(\frac{1}{W_1} + \frac{3}{W_2}\right) = \frac{L_{min}^2}{\mu_n (V_{DD} - V_T)}\left(4 + \frac{W_2}{W_1} + 3\frac{W_1}{W_2}\right)$$

For min size:	For equal rise/fall:	For min delay:
$W_2 = W_1 = W_{min}$	$W_2 = 3W_1$	$W_2 = \sqrt{3} W_1$
$t_{PROP} = \frac{8L_{min}^2}{\mu_n (V_{DD} - V_T)}$	$t_{PROP} = \frac{8L_{min}^2}{\mu_n (V_{DD} - V_T)}$	$t_{PROP} = \frac{(4 + 2\sqrt{3})L_{min}^2}{\mu_n (V_{DD} - V_T)}$

$\left(4 + 2\sqrt{3}\right) \cong 7.5$

Propagation Delay About the Same for 3 Sizing Strategies

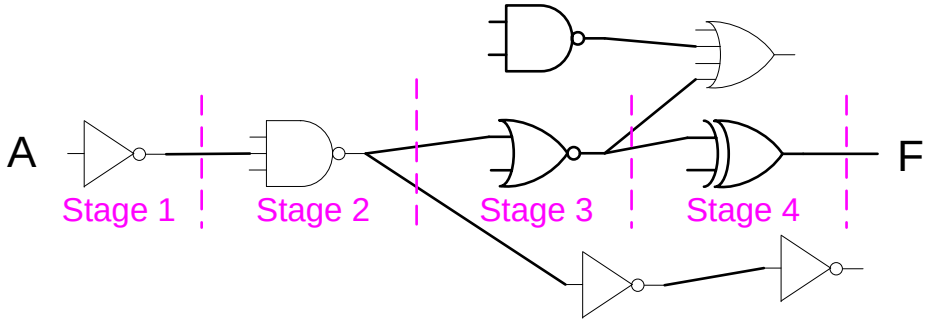
Propagation Delay in Static CMOS Family



The propagation delay through k levels of logic is approximately the sum of the individual propagation delays in the same path

Propagation Delay in Static CMOS Family

Example:



$$t_{HL}=t_{HL4}+t_{LH3}+t_{HL2}+t_{LH1}$$

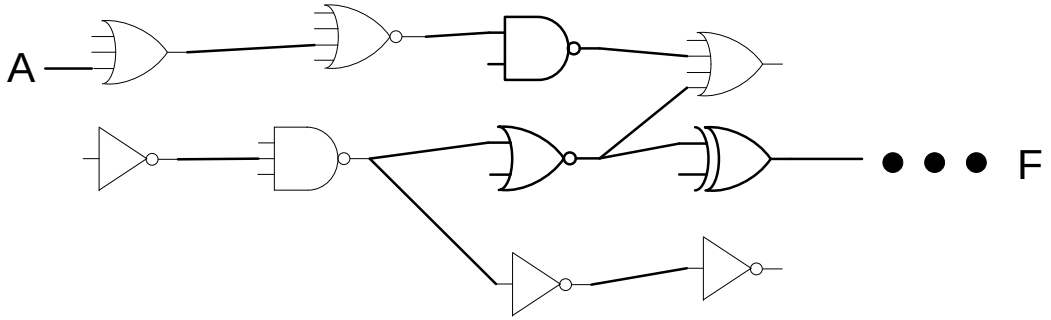
$$t_{LH}=t_{LH4}+t_{HL3}+t_{LH2}+t_{HL1}$$

$$t_{PROP}=t_{LH}+t_{HL}=(t_{LH4}+t_{HL3}+t_{LH2}+t_{HL1})+(t_{HL4}+t_{LH3}+t_{HL2}+t_{LH1})$$

$$t_{PROP}=t_{LH}+t_{HL}=(t_{LH4}+t_{HL4})+(t_{LH3}+t_{HL3})+(t_{LH2}+t_{HL2})+(t_{LH1}+t_{HL1})$$

$$t_{PROP}=t_{PROP4}+t_{PROP3}+t_{PROP2}+t_{PROP1}$$

Propagation Delay in Static CMOS Family



Propagation through k levels of logic

$$t_{HL} \cong t_{HLk} + t_{LH(k-1)} + t_{HL(k-2)} + \bullet\bullet\bullet + t_{XY1}$$

$$t_{LH} \cong t_{LHk} + t_{HL(k-1)} + t_{LH(k-2)} + \bullet\bullet\bullet + t_{YX1}$$

where X=H and Y=L if k odd and X=L and Y=h if k even

$$t_{PROP} = \sum_{i=1}^{k} t_{PROPk}$$

Will return to propagation delay after we discuss device sizing

Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
    - FI/OD
    - Logical Effort
  - Elmore Delay
- Sizing of Gates
  - The Reference Inverter

- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators

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done

partial

Observation:

$|V_{Tp}| \approx V_{Tn} \approx V_{DD}/5$ in many processes

Question:

?

?

?

?

?

Why is $|V_{Tp}| \approx V_{Tn} \approx V_{DD}/5$ in many processes ?

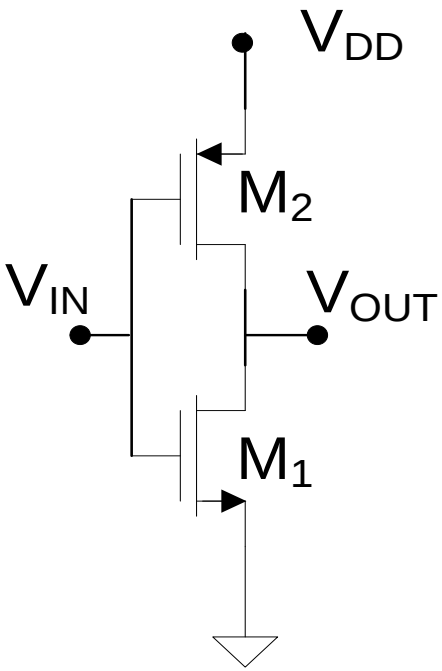
?

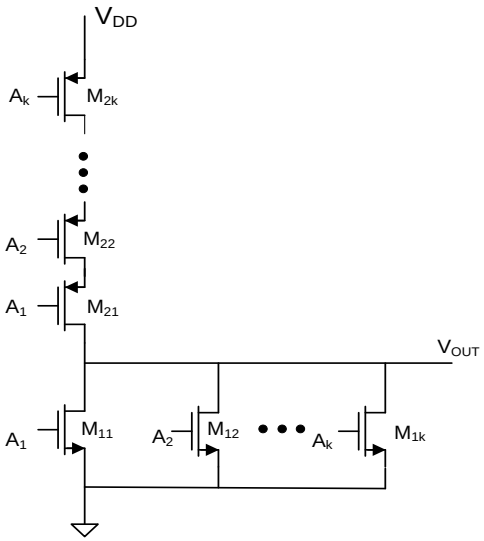
?

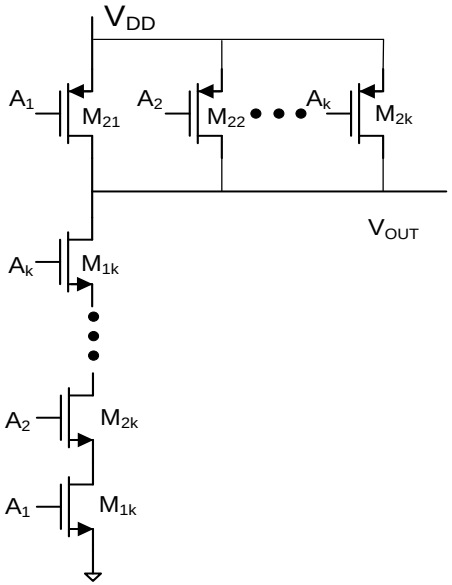
?

?

Device Sizing





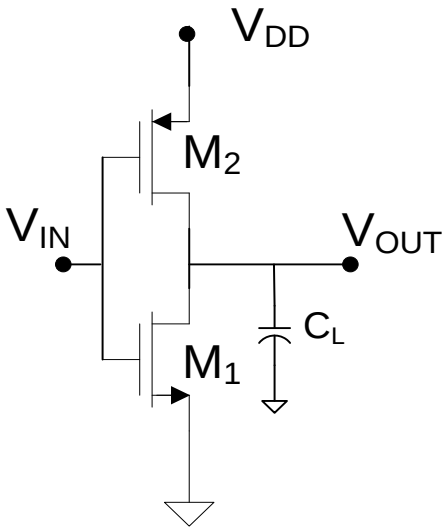


Strategies?

Degrees of Freedom?

Will consider the inverter first

Device Sizing

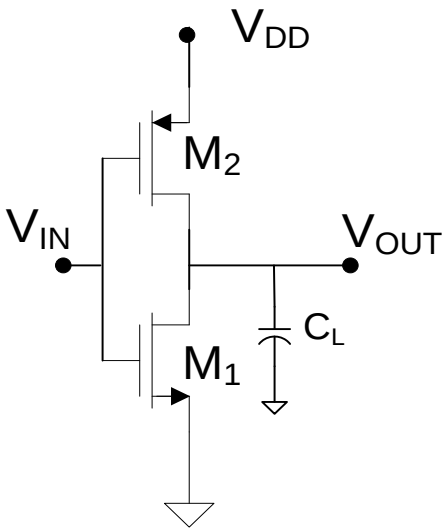


Degrees of Freedom?

Strategies?

Device Sizing

- **Since not ratio logic, V_H and V_L are independent of device sizes for this inverter**
- **With $L_1=L_2=L_{min}$, there are 2 degrees of freedom (W_1 and W_2)**

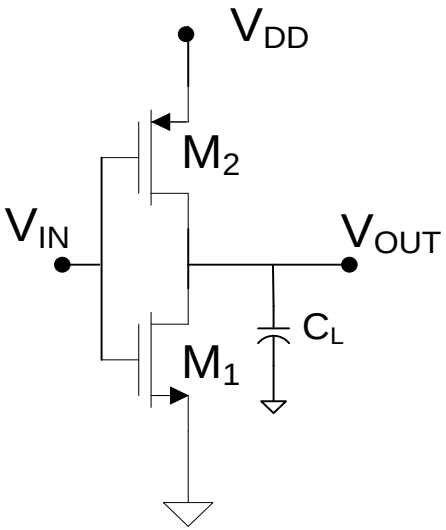


Sizing Strategies

- **Minimum Size**
- **Fixed V_{TRIP}**
- **Equal rise-fall times (equal worst-case rise and fall times)**
- **Minimum power dissipation**
- **Minimum time required to drive a given load**
- **Minimum input capacitance**

Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{min}$



Sizing Strategy: minimum sized

W_n=?, W_p=?, V_{trip}=?,t_{HL}=?,t_{LH}=?

$$R_{PD} = \frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_{Tn})}$$

$$R_{PU} = \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} + V_{Tp})}$$

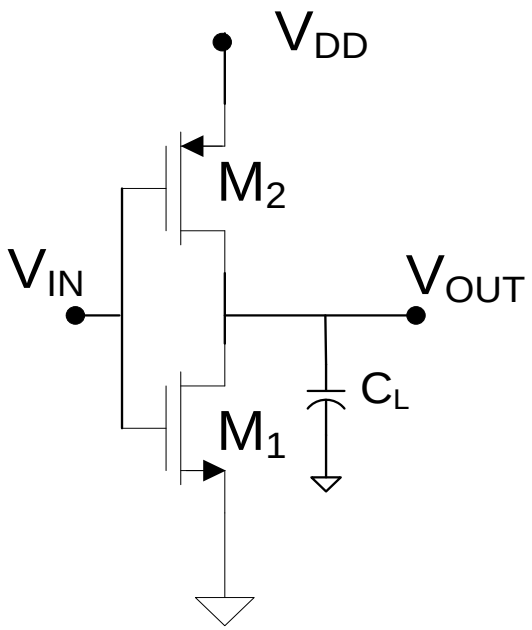
$$C_{IN} = C_{OX}(W_1 L_1 + W_2 L_2)$$

Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{min}$

Sizing Strategy: minimum sized

W_n=?, W_p=?, V_{trip}=?,t_{HL}=?,t_{LH}=?



$W_1=W_2=W_{MIN}$

also provides minimum input capacitance

It follows that $R_{PU}=\mu_n/\mu_p R_{PD}$

$t_{HL}=R_{PD}C_L$

$t_{LH}=3\ R_{PD}C_L$

t_{LH} is longer than t_{HL}

$t_{PROP}=4R_{PD}C_L$

$$V_{TRIP}=\frac{(V_{Tn})+(V_{DD}+V_{Tp})\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}{1+\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}$$

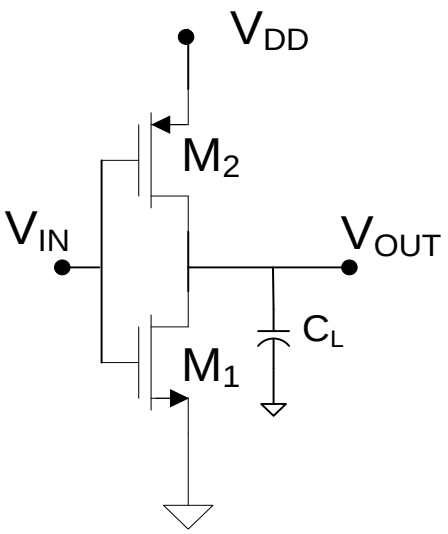
$$V_{TRIP}=\frac{(0.2V_{DD})+(V_{DD}-0.2V_{DD})\sqrt{\frac{1}{3}}}{1+\sqrt{\frac{1}{3}}}=.42V_{DD}$$

Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{min}$

Sizing strategy: Equal (worst case) rise and fall times

W_n=?, W_p=?, V_{trip}=?,t_{HL}=?,t_{LH}=?



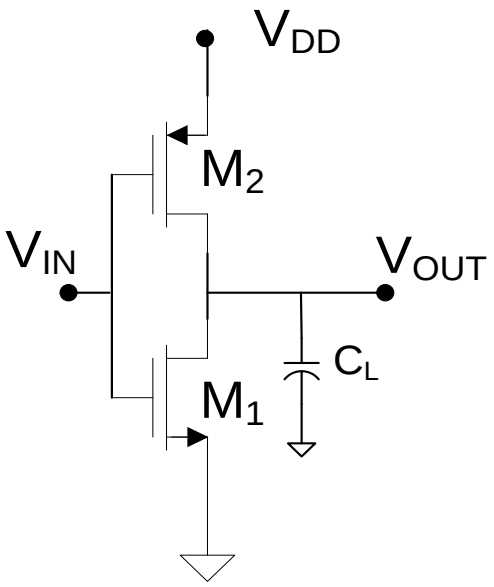
$$R_{PD} = \frac{L_{min}}{\mu_n C_{OX} W_1 (0.8V_{DD})}$$

$$R_{PU} = \frac{L_{min}}{3\mu_n C_{OX} W_2 (0.8V_{DD})}$$

Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{min}$

Sizing strategy: Equal (worst case) rise and fall times



$$\frac{t_{LH}}{t_{HL}}=1=\frac{R_{PU}C_{IN}}{R_{PD}C_{IN}} \Rightarrow R_{PU}=R_{PD}$$

Thus

$$\frac{L_1}{u_nC_{OX}W_1\left(V_{DD}-V_{Tn}\right)}=\frac{L_2}{u_pC_{OX}W_2\left(V_{DD}+V_{Tp}\right)}$$

with $L_1=L_2$ and $V_{Tp}=-V_{Tn}$ we must have

$$\frac{W_2}{W_1}=\frac{\mu_n}{\mu_p}\cong 3$$

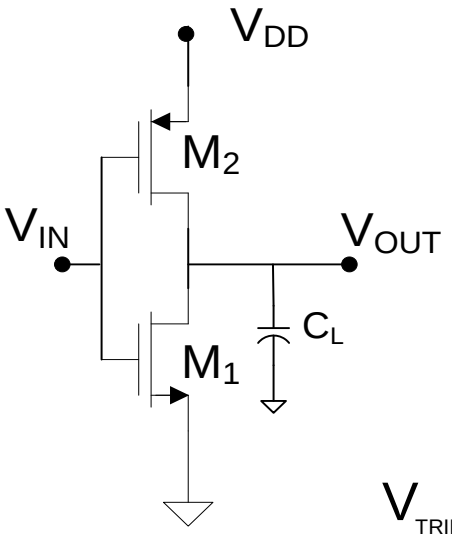
What about the second degree of freedom?

$W_1=W_{MIN}$ **(could be something else)**

$V_{TRIP}=?$

Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{min}$



Sizing strategy: Equal (worst-case) rise and fall times

$W_n=W_{MIN}, W_p=3W_{MIN}$, $V_{trip}=?, t_{HL}=?, t_{LH}=?$

$$V_{TRIP} = \frac{(V_{Tn}) + (V_{DD}+V_{Tp})\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}{1+\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}} = \frac{0.2V_{DD}+0.8V_{DD}}{2} = \frac{V_{DD}}{2}$$

$$t_{HL} = t_{LH} = R_{pd}C_L = \frac{L_{min}}{\mu_n C_{OX} W_{min}(0.8V_{DD})} C_L$$

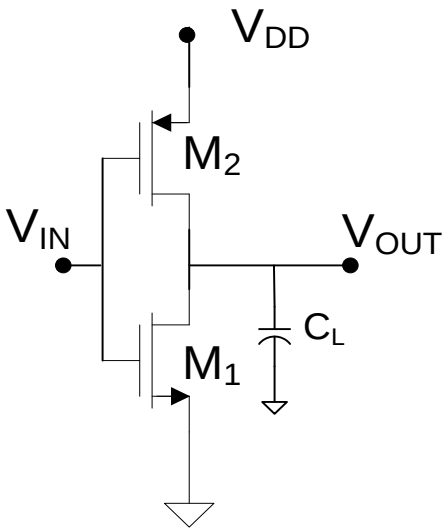
$$t_{PROP} = 2\,R_{pd}C_L$$

For a fixed C_L, how does t_{prop} compare for the minimum-sizing compared to equal rise/fall sizing?

Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{min}$

Sizing strategy: Fixed $V_{TRIP}= V_{DD}/2$ (Could have other V_{TRIP})



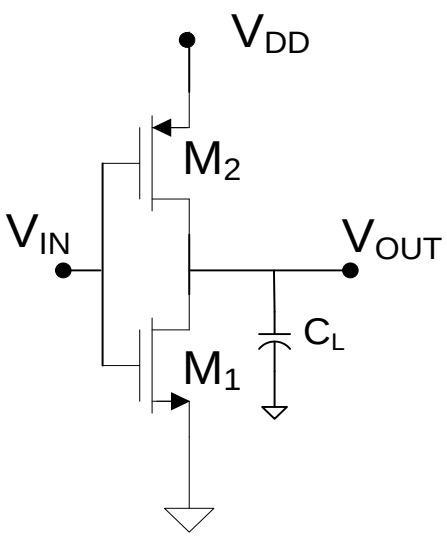
W_n=?, W_p=?, V_{trip}=?,t_{HL}=?,t_{LH}=?

Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{min}$

Sizing strategy: Fixed $V_{TRIP}=V_{DD}/2$

W_n=?, W_p=? , V_{trip}=?,t_{HL}=?,t_{LH}=?



Set

$V_{TRIP}=V_{DD}/2$

$$V_{TRIP}=\frac{(.2V_{DD})+(V_{DD}-.2V_{DD})\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}{1+\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}=\frac{V_{DD}}{2}$$

Solving, obtain

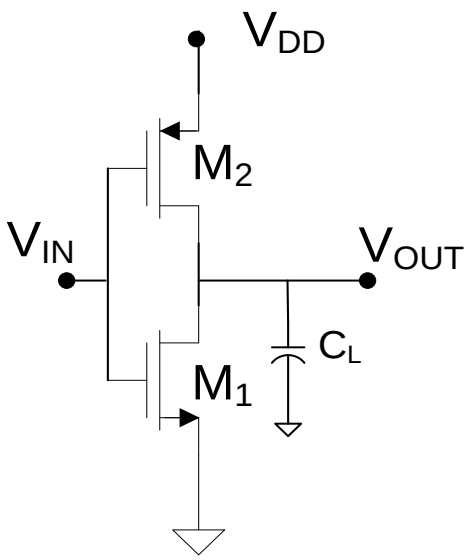
$$\frac{W_2}{W_1}=\frac{\mu_n}{\mu_p}$$

$W_n=W_{MIN}$, $W_p=3W_{MIN}$

- **This is the same sizing as was obtained for equal worst-case rise and fall times so $t_{HL}=t_{LH}=R_{pd}C_L$**
- **This is no coincidence !!! Why?**
- **These properties guide the definition of the process parameters provided by the foundry**

Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{min}$



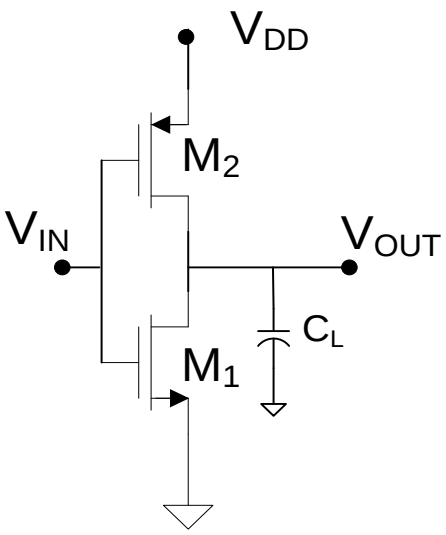
Sizing Strategies

- **Minimum Size**
- **Fixed V_{TRIP} ($V_{TRIP}=V_{DD}/2$)**
- **Equal rise-fall times (equal worst-case rise and fall times)**
- **Minimum power dissipation**
- **Minimum time required to drive a given load**
- **Minimum input capacitance**

Device Sizing

Assume $V_{Tn}=0.2V_{DD}$, $V_{Tp}=-0.2V_{DD}$, $\mu_n/\mu_p=3$, $L_1=L_2=L_{min}$

Sizing Strategy Summary



	Minimum Size	$V_{TRIP}=V_{DD}/2$	Equal Rise/Fall
Size	$W_n=W_p=W_{min}$ $L_p=L_n=L_{min}$	$W_n=W_{min}$ $W_{p=}3W_{min}$ $L_p=L_n=L_{min}$	$W_n=W_{min}$ $W_{p=}3W_{min}$ $L_p=L_n=L_{min}$
t_{HL}	$R_{pd}C_L$	$R_{pd}C_L$	$R_{pd}C_L$
t_{LH}	$3R_{pd}C_L$	$R_{pd}C_L$	$R_{pd}C_L$
t_{PROP}	$4R_{pd}C_L$	$2R_{pd}C_L$	$2R_{pd}C_L$
V_{trip}	$V_{TRIP}=0.42V_{DD}$	$V_{TRIP}=0.5V_{DD}$	$V_{TRIP}=0.5V_{DD}$

- **For a fixed load C_L, the minimum-sized structure has a higher t_{PROP} but if the load is another inverter, C_L will also change so the speed improvements become less apparent**
- **This will be investigated later**

Question:

Why is $|V_{Tp}| \approx V_{Tn} \approx V_{DD}/5$ in many processes ?

Stay Safe and Stay Healthy !

End of Lecture 39